

**INSTALLATION AND SERVICE
MANUAL**

**HP 91200B
TV INTERFACE KIT**

Manual part no. 91200-90001
Microfiche part no. 91200-90002

Printed: NOV 1976

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Card Assembly 91200-60007

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Change 0 (Original) Nov 1976

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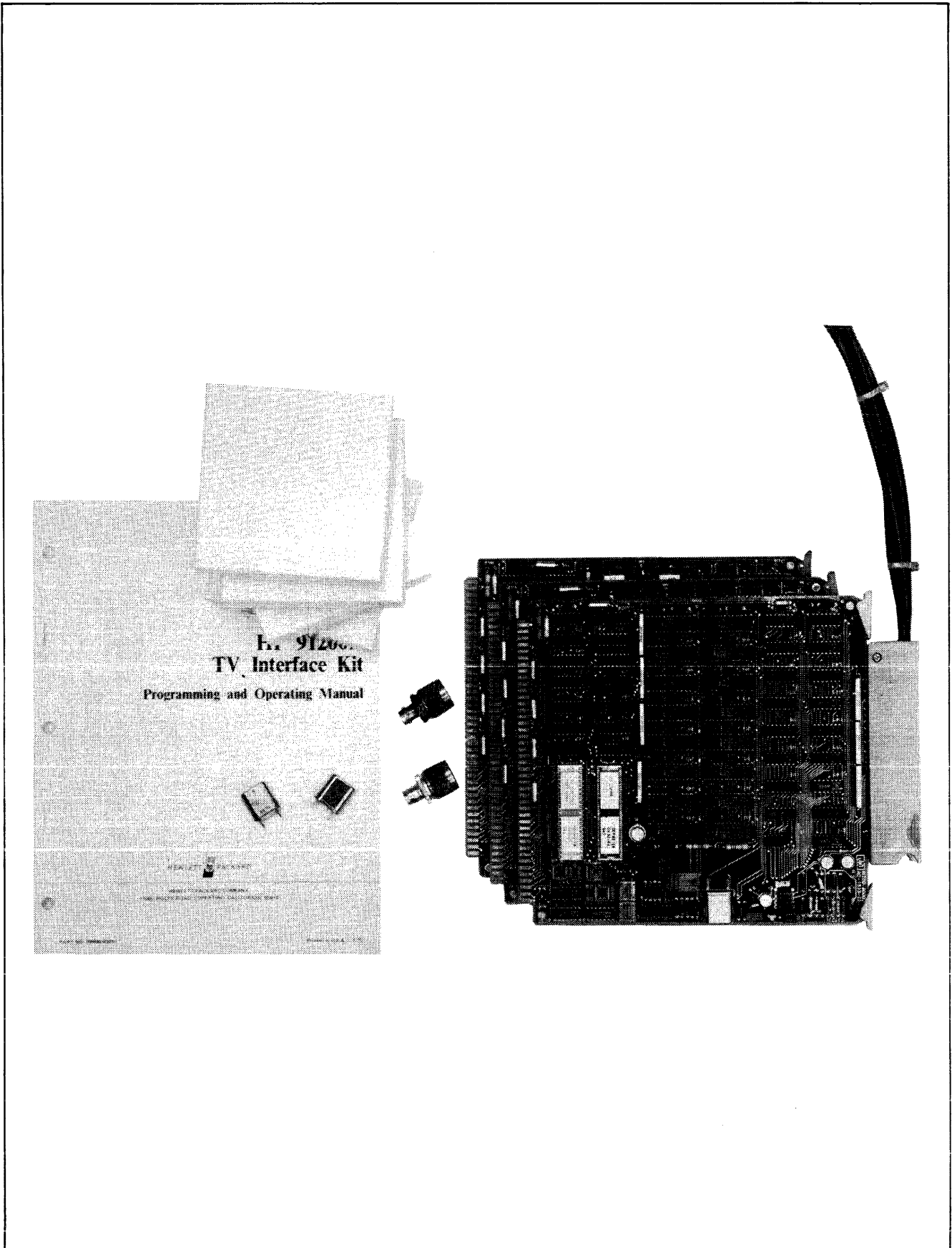
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Figure 1-1. HP 91200B TV Interface Kit with Options

GENERAL INFORMATION

SECTION

I

1-1. INTRODUCTION

1-2. This manual contains general information, installation instructions, a functional description, and service instructions for the Hewlett-Packard 91200B TV Interface Kit. The kit is shown in figure 1-1 along with optional crystals, software, cable adapters, and cards with triple-hooded output connector for color or multiple gray level operation. The basic kit includes the TV interface card assembly, output connector assembly, diagnostic software tape, and this installation and service manual. Other required or accessory items are options to the HP 91200B Kit. Refer to paragraphs 1-14 and 1-16 for listings of equipment supplied and options, respectively.

1-3. The HP 91200B TV Interface Kit is compatible with the HP 2100A/S and HP 21MX Computers. The TV Interface Software is described in the *HP 91200B TV Interface Kit Programming and Operating Manual*, part no. 91200-90006.

1-4. GENERAL DESCRIPTION

1-5. A single TV interface card can be programmed to provide displays which combine both graphic images and alphanumeric characters on standard television monitors. Systems having two or three cards can display variable levels of gray on black and white (BW) monitors or color on color tube monitors. The monitors should be designed for EIA RS-170 composite video signals. The card video and sync outputs are designed to drive up to five monitors, connected in series, through 75-ohm coaxial cable. The furthest monitor can be up to 500 meters (1640 ft) away from the computer.

1-6. The display information of up to 65,536 individually addressable bits is stored on the card in Random Access Memory (RAM). A 256 by 256 dot matrix format is used. All points of the display are covered in a single complete TV scan using the card generated sync and the RAM point-by-point picture information. Because of the RAM, no CPU time is needed to refresh the display.

1-7. There are three modes of scan operation available which are selected by jumpers and the scan oscillator crystal. Mode I is the American Broadcast Standard of 525 lines-per-frame at 60 fields-per-second. Mode II is the European Broadcast Standard of 625 lines-per-frame at 50 fields-per-second. Mode III is a non-standard scan of 288 lines-per-frame and 60 frames or fields-per-second. Mode I and Mode II have a 2:1 interlace and Mode III is without interlace. Mode I uses a 256 by 240 data matrix and Modes II and III use the full 256 by 256 data matrix. The Ameri-

can and European modes can be operated without interlace if it is not necessary to be compatible with broadcast video systems. For interlaced scans, the second scan can be a duplicate of the first or it can be blanked. Scan specifications are covered in table 1-1.

1-8. The user can program the TV interface card with FORTRAN, ALGOL, Real-Time BASIC and Assembly language calls to generate different sized characters, vectors, and illuminated areas as well as to erase and update any portion of the picture without having to reenter the entire displayed information. The card is supported in memory-based RTE-B and RTE-C operating systems and disc-based RTE operating systems.

1-9. The user can program for control of gray scale or color when multiple TV interface cards are installed in the system. For color, using a color monitor, a separate card is required for each of the red, green, and blue primary screen colors to be used. Three cards can provide displays of six saturated colors plus white and black on a color monitor; or eight levels of black and white from 7/8ths white to black on a BW monitor. Two cards can provide displays of three saturated colors plus black on a color monitor, or 1/2 and 3/4ths white and black on a BW monitor.

1-10. Synchronization and video amplification is provided on the cards. In multiple card operation for gray scale on a BW monitor, the raw video outputs are summed on a master card to provide a composite signal with sync. To maintain sync on all cards providing video to the master card, the clock signal of the master card (designated card A) is forwarded to slave cards (designated as cards B and C). A separate sync signal is provided for TV monitors which have difficulty synchronizing to a composite video signal. Industry standard synchronization in the TV interface card enables the user to mix the card generated video with other video signals to create split-screen effects and composite TV pictures.

1-11. The display may be program written as either white on black background or black on a white background. The stored image is reversible by changing one bit so the user can easily select either way. This causes the display to flash back and forth as an attention getter without loss of message. The same bit will cause all colors to change to their complements if switched to its opposite state; i.e., red becomes cyan, blue becomes yellow, etc.

1-12. Figure 1-2 is a simplified block diagram of the TV interface card. The memory section stores the data for output to the display. The section is composed of an input register, mode register, multiplexer, memory address register, RAM select storage, RAM select decoder, and the

random access memory (RAM). A 16-bit computer word is used to address any point in memory. The timing section produces the timing, blanking, and sync pulses for card and display operation. The control section contains the logic necessary for communication with the computer and also controls the memory section. The video section converts the memory output from parallel to serial form and provides sync and video outputs.

1-13. The address of the displayed point is available to the user at the instant it is scanned to facilitate the addition of a light pen. The lower 8-bit byte addresses the X (horizontal) axis of 256 locations and the upper 8-bit byte addresses the Y (vertical) axis of 256 locations. Address "0,0" is displayed on the lower left-hand corner of the monitor screen.

1-14. EQUIPMENT SUPPLIED

- 1-15. The basic kit contains the following:
- a. TV Interface Card Assembly, part no. 91200-60007.
 - b. TV Interface Diagnostic Tape, part no. 91200-16003.
 - c. Connector Assembly, part no. 02313-60010.
 - d. *HP 91200B TV Interface Kit Installation and Service Manual*, part no. 91200-90001.

Table 1-1. Specifications

Operating System Compatibility	Supported for use in RTE-B, RTE-C, RTE-II and RTE-III operating systems only.		
Electrical			
Power Consumption (max.)	+5V @ 1.2A, -2V @ 0.05A, +12V @ 0.32A, -12V @ 0.05A		
Output Impedance	75 ohms		
Video Polarity	Programmable		
Video Levelst			
White	0 volt	} composite video from 75Ω source	
Black	-1 volt (approx.)		
Sync	-1.4 volts		
Ext. Sync Level	4.0 volts negative-going pulse (nominal)		
Operating Modes	American I	European II	Non-Standard III
Lines per Frame	525	625	288
Lines per Field	262.5**	312.5**	288
Fields per Frame	2	2	1
Fields per Second	60	50	60
Interlace	2:1**	2:1**	none
Lines of Data per Field	240	256	256
Horizontal Scan Rate	15,750 Hz	15,625 Hz	17,281.25 Hz
Point Rate	5.040 MHz	5.000 MHz	5.530 MHz
Crystal Oscillator Frequency‡	10.080 MHz	10.000 MHz	11.060 MHz
Frames per Second	30**	25**	60
TV Monitors	Up to five monitors may be connected to one TV interface card.		
Maximum Cable Length	500 meters (1640 feet)		
Environmental Operating Conditions	0° to 55°C (32° to 131°F)*, same as for HP 2100A/S and HP 21MX Computers; up to 15°C (27°F) should be allowed for temperature rise inside HP system cabinets.		
Physical			
Weight	Shipping 1.82 kg (4 lbs)		
Dimensions	220.7 mm (8-11/16 in.) x 196.9 mm (7-3/4 in.)		
<p>*Temperature range outside computer. **American and European modes may be operated without interlace if it is not necessary to be compatible with broadcast video systems. † The specified voltage levels have a tolerance of ±5% on the peak-to-peak value of the composite video signal when driving a 75-ohm load. ‡ +0.05%, thus providing this general tolerance to all time and frequency specifications.</p>			

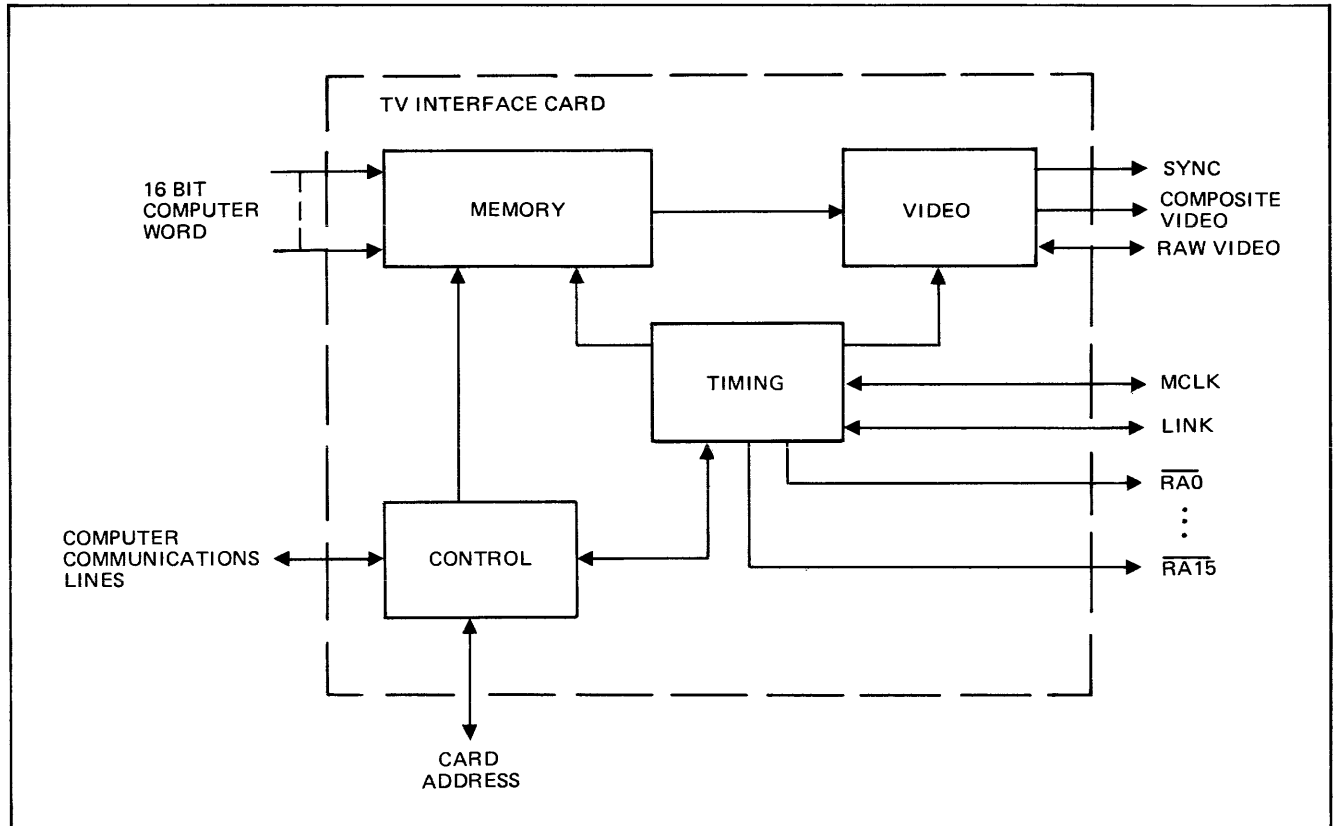


Figure 1-2. Simplified Block Diagram

1-16. OPTIONS

1-17. Options are available to allow configuration flexibility. These options are described below:

a. Option 442 Software Package:

- RTE Driver DVA13 Binary Tape, part no. 91200-16001.
- DVA13 Manual, part no. 91200-90005.
- TV Interface Library Tape, part no. 91200-16002.
- TV Interface Verification Tape, part no. 91200-16004.
- Programming and Operating Manual, part no. 91200-90006.

b. Option 001, Coaxial Cable Assembly for single cards:

- Coaxial Cable Assembly, part no. 91200-60006.
- Coaxial Connector Adapters (2), BNC to UHF, part no. 1250-0071.
- Removes connector assembly 02313-60010 from basic kit.

c. Option 003, Coaxial Cable Assembly for triple cards:

- Coaxial Cable Assembly, part no. 91200-60008.
- Coaxial Connector Adapters (4), BNC to UHF, part no. 1250-0071.
- Removes connector assembly 02313-60010 from basic kit.

d. Option 010, Quartz Crystal for American Scan:

- Crystal for 10.0800 MHz, part no. 0410-0592.

e. Option 011, Quartz Crystal for Non-Standard Scan:

- Crystal for 11.0600 MHz, part no. 0410-0591.

f. Option 015, Quartz Crystal for European Scan:

- Crystal for 10.0000 MHz, part no. 0410-0035.

1-18. IDENTIFICATION

1-19. The TV interface card is identified by a part number and a revision code (see figure 2-1). The ten-digit part number 91200-60007 is the same for all cards. The revision code consists of a letter, a series code, and a

division code (e.g., A-1503-22). The letter code identifies the version of the etched trace pattern on the unloaded board. The series code (four middle digits) refers to the electrical characteristics of the loaded assembly and the positions of the components. The division code (last two digits) identifies the Hewlett-Packard division that manufactured the card. Cards having the same part number but different revision codes are interchangeable unless noted otherwise in this manual or by a manual supplement. Manual supplements are available from HP Sales and Service Offices (see list at the back of this manual).

1-20. SPECIFICATIONS

1-21. Table 1-1 lists the major electrical, environmental, and physical specifications of the TV interface card.

1-22. CARD REPAIR

1-23. The TV interface card is a field replaceable item and should be maintained on an exchange basis. To verify card operation within an RTE environment, use the on-line RTE verification procedure given in the programming and operating manual; otherwise, perform the off-line diagnostic test given in Section IV. If a malfunction is confirmed by the diagnostic, the card should be replaced with an exchange assembly. The exchange card, part no. 91200-69007, is available at a reduced rate. The nearest Hewlett-Packard Sales and Service Office can provide all procurement details.

2-1. INTRODUCTION

2-2. This section provides installation instructions which includes recommended procedures on preparing the TV interface card for operation with the computer in the user's system. Card installation instructions include unpacking and initial inspection, cable preparation, and card installation. Single cards, multiple cards for gray scale and for color are covered.

2-3. UNPACKING AND INITIAL INSPECTION

2-4. Any shipping container that appears damaged should be unpacked with the carrier's agent present. Carefully inspect the TV interface card for damage, scratches, cracks, etc. Check that all equipment specified in the purchase order has been delivered; refer to Section I for the list of components supplied with the kit. If any equipment is missing, damaged, or fails to meet specifications, immediately notify the carrier and the nearest Hewlett-Packard Sales and Service Office listed at the back of this manual. Retain the shipping containers and packing material for the carrier's inspection and for future use.

2-5. USER PREREQUISITES

2-6. TV MONITOR REQUIREMENTS

2-7. The customer must provide a suitable TV monitor designed for EIA RS-170 composite video signals. The monitor input should match a 75-ohm source impedance. Refer to table 1-1 for operating mode specifications. For Mode III, the monitor must be capable of synchronizing to a horizontal rate of 17,280 Hz and a vertical rate of 60 Hz. For Mode II the monitor must sync at a horizontal rate of 15,625 Hz and a vertical rate of 50 Hz. For Mode I, the American broadcast standard, the horizontal sync rate is 15,750 Hz and the vertical rate is 60 Hz. The TV sets or studio monitors operated from the TV interface card may be equipped with a composite video input or separate picture and sync inputs. The sets or monitors should sync properly if designed for the sync rates of the card operating mode. For best dot definition, it is desirable that the monitor have a video bandwidth of 8 MHz or more. Additional desirable features are good linearity, dc restoration, dc sync pick-off or external sync input, non-glare screen, and wide-range high-voltage regulation. If more than one monitor is to be used with one card, it is necessary that the monitor have chaining connectors, and be able to switch from a 75-ohm termination to a high impedance. In operation,

a slight "underscan" of the monitor screen is desirable so that the entire display is visible.

2-8. CABLES

2-9. The user shall furnish 75-ohm coaxial chaining cables (e.g., RG-59/U or RG-59B/U) for the connection of extra monitors or for additional cable lengths. The last monitor should have no more than 500 meters (1640 feet) of cable between it and the TV interface card. A coaxial cable pair, 7.5 meters (25 feet) long is furnished with option 001. Option 003 includes three video cables and one sync cable, all 7.5 meters (25 feet) long. The cables are connected into a triple-hooded edge connector for three TV interface cards. Lengths of cable may be joined by using straight female-to-female couplers. BNC to UHF (PL-259) plug adapters are furnished for each cable (with options 001 and 003) to mate with monitors having UHF (SO-239) type chassis receptacles. If the composite video/sync signal is used, the separate sync cable will not be necessary. It may be rolled up and stored at the rear of the equipment in case it may be needed at some time in the future.

2-10. INSTALLATION

2-11. BLACK-AND-WHITE OPERATION

2-12. The following procedure describes how to install a single TV interface card for black-and-white (BW) operation. The procedure is as follows:

- a. Determine if the computer power supply will provide the additional current required for operation of the TV interface card. The power required is given in table 1-1, specifications. If the addition of the card will overload the computer power supply, an appropriate computer I/O extender must be used. (HP 2100A/S and HP 21MX Computers work with HP 2155A and HP 12979A I/O Extenders, respectively.)

Note: If the TV interface card is to be used in a system under DMA (or DCPC) control, the card must be installed in a computer mainframe having DMA (or DCPC). The card could also be operated in an I/O extender having DMA (or DCPC) as long as the computer also has the DMA (or DCPC) capability. An RTE environment requires DMA (or DCPC).

- b. Determine mode of operation. Refer to table 2-1 which describes the functions of the jumpers on the TV interface card for the three scanning modes. Jumper location is shown in figure 2-1.
- c. Install crystal after making sure it is the right one for scanning mode selected (see table 2-1).
- d. Set jumpers for single or multiple card operation. Refer to table 2-2 for jumper positions. Refer to figure 2-1 for location of jumpers. Place unused jumpers in the jumper storage socket on the card for future use.
- e. When fabricating cable assemblies, use the hooded connector, part no. 02313-60010, supplied with each HP 91200B Kit unless this item was deleted by the use of one of the cable assembly options (001 and 003). Construction details are shown in figure 2-2.
- f. If two or more monitors are to be connected to the TV interface card, fabricate cables to link them together from the first monitor. Use RG-59/U or RG-59B/U 75-ohm coaxial cable and appropriate connectors to mate with the monitor connectors.

CAUTION

Always make sure that the computer power is in either *standby* for HP 21MX or *off* for HP 2100A/S Computers when installing or removing the interface card or interconnecting cable. Failure to observe this caution may damage the card.

- g. Insert card in the computer card cage in the following manner:
 - (1) Turn computer power to standby (HP 21MX) or off (HP 2100A/S) and gain access to I/O card cage.
 - (2) Hold card vertically with components on the left for the HP 2100A/S Computers. Hold card horizontally with components up for the HP 21MX Computer and the HP 12979A I/O Extender. Plastic card extractors should face away from the computer.
 - (3) Carefully slide card into its assigned slot.
 - (4) Seat card fully in its mating backplane receptacle by pressing firmly inward on its card extractors.
- h. To install the 7.5 meter (25 ft) cable and hood assembly on the card(s) in the computer or I/O extender, proceed as follows:
 - (1) For the HP 2100A/S Computer, orient the hood so that the cable exits towards the rear of the cabinet. For the HP 21MX Computer and rear of the HP 12979A I/O Extender, orient the hood so

the cable exits toward the right side when facing the rear of the cabinet. For the HP 12979A I/O Extender front access, orient the hood so the cable exits the hood towards the right. The cable should run up the right cabinet wall and cross over to the left side then out the rear cable port.

- (2) Carefully slide cable hood connector onto the 48-pin edge connector of the card and press into place.
- (3) Connect VIDEO connector to the TV monitor. Note that some monitors may also require connection of the SYNC output (see paragraph 4-23).

Note: It is the user's responsibility to provide an appropriate TV monitor in good operating condition. The diagnostic and verification tests require that the TV monitor be connected to the card.

2-13. After installation, a performance check can be made in one of two ways. For off-line checking, use the diagnostic test procedure described in Section IV. For RTE on-line checking (except for RTE-B operating systems), use the verification program described in the *HP 91200B TV Interface Kit Programming and Operating Manual*, part no. 91200-90006. The verification and diagnostic programs provide a convenient means of checking the TV monitor's adjustments. The RTE software operating system must be generated for the verification test to function.

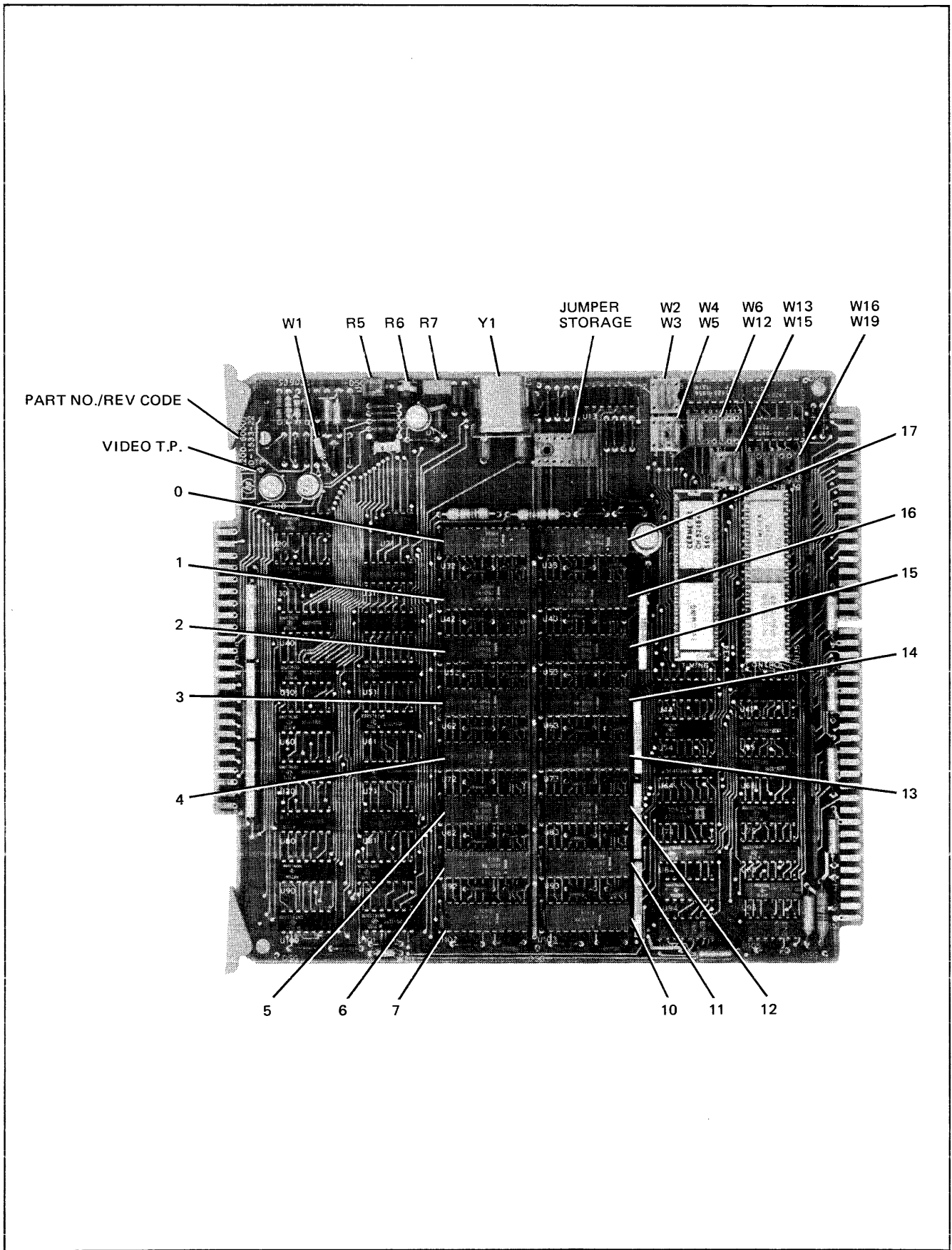
2-14. COLOR MONITOR OPERATION

2-15. Color monitors require a separate TV interface card for each color input of a color CRT. For this application, three cards are used with one option 003 triple-hooded connector. Two color inputs require two cards and two part no. 02313-60010 hooded connectors (supplied with the basic kit) with connectors and cables fabricated according to figures 2-2 and 2-4. The cards should sit side-by-side in either the computer I/O card cage or I/O extender. The master card (designated as card A) must be placed in the highest numbered slot of the group and will be addressed by the select code (or LU number in RTE systems) assigned to the TV interface subsystem. The master card is followed in descending order by slave card B and slave card C. Perform the following procedures to install a set of cards for color operation:

- a. Review the black-and-white operation installation procedure given in paragraph 2-11. Observe the power supply and current requirements of the cards and other considerations such as I/O with DMA (or DCPC) and all cautions and notes.
- b. The wiring of three-card cables and the triple PC card connector for color is shown in figure 2-4, using option 003. Two card setups, using single hoods, should be wired according to figure 2-4 with card C deleted and the hoods assembled as shown in figure 2-2.

Table 2-1. Scanning-Mode Jumper Positions

AMERICAN STANDARD (MODE I)	
JUMPER	DISPLAY OR USE
W2-A W3-A W3-B W4-X W5-A W6-IN W6-OUT W7-OUT W8-IN W9-IN W9-OUT W10-OUT W11-IN W11-OUT W12-IN	American Standard. Single or master card clock enable. Slave card (B and C) clock disable, external clock connect. American Standard - not used (don't care). American Standard. Horizontal display points defined. Horizontal lines, points undefined. American Standard. American Standard. Interlace enabled (2 fields, 525 lines). Interlace disabled (1 field, 524 lines). American Standard. Second field blanked (262.5 lines with W9-IN, 262 lines with W9-OUT). Both fields. American Standard.
EUROPEAN STANDARD (MODE II)	
JUMPER	DISPLAY OR USE
W2-B W3-A W3-B W4-A W5-B W6-IN W6-OUT W7-IN W8-IN W9-IN W9-OUT W10-IN W11-IN W11-OUT W12-OUT	Sync. Single or master card clock enable. Slave card (B and C) clock disable, external clock connect. Timing. Timing. Horizontal display, points defined. Horizontal display, points undefined. Timing. Timing. Timing. Interlaced (2 fields, 625 lines). Interlace disabled (1 field, 624 lines). Sync 2nd field blanked (312.5 lines with W9-IN, "don't care" with W9-OUT). Both fields with W9-IN, "don't care" with W9-OUT. Sync.
NON-STANDARD (MODE III)	
JUMPER	DISPLAY OR USE
W2-B W3-A W3-B W4-B W5-B W6-IN W6-OUT W7-IN W8-OUT W9-OUT W10-IN W11-IN W11-OUT W12-OUT	Sync. Single or master card clock enable. Slave card (B and C) clock disable, external clock connect. Timing. Timing. Horizontal display, points defined. Horizontal display, points undefined. Timing. Timing. Timing. 1 field of 288 lines. Sync. Don't care. Don't care. Sync.
CRYSTALS Mode I American Standard. 10.080 MHz, part no. 0410-0592. Mode II European Standard. 10.000 MHz, part no. 0410-0035. Mode III Non-standard. 11.060 MHz, part no. 0410-0591.	



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Figure 2-1. TV Interface Card

- c. Place a small strip of tape on each card and label them A, B, and C for master, slave 1, and slave 2, respectively.
- d. Set jumpers on cards according to table 2-1 for scanning requirements and table 2-2 for multiple card operation.

Table 2-2. Single or Multiple-Card Jumper Positions

JUMPER	DESCRIPTION OF USE
W1-A	Black-and-white or color (solder-in type).
W1-B	Multi-level gray.
W13-A	Single or master card (card A).
W13-B	Slave card (cards B and C).
W14-IN	Single or master card (card A).
W14-OUT	Slave card (cards B and C).
W15-IN	Single or master card (card A).
W15-OUT	Slave card (cards B and C).
W16-A	Single or master card (card A).
W16-B	Slave card (cards B and C).
W17-IN	Single or master card (card A).
W17-OUT	Slave card (cards B and C).
W18-A	Single or master card (card A).
W18-B	Slave card B (first slave).
W18-C	Slave card C (second slave).
W19-IN	Single or master card (card A).
W19-OUT	Slave card (cards B and C).
W20	For factory use only (solder-in type).

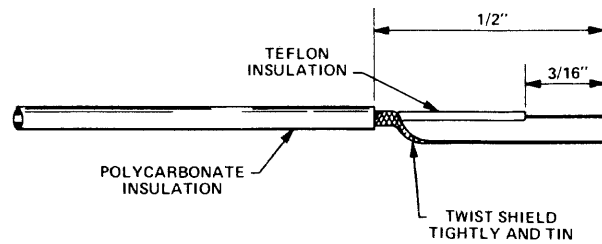
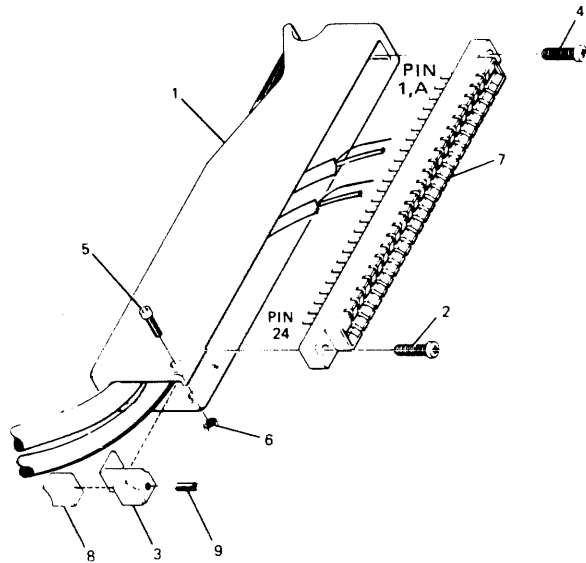
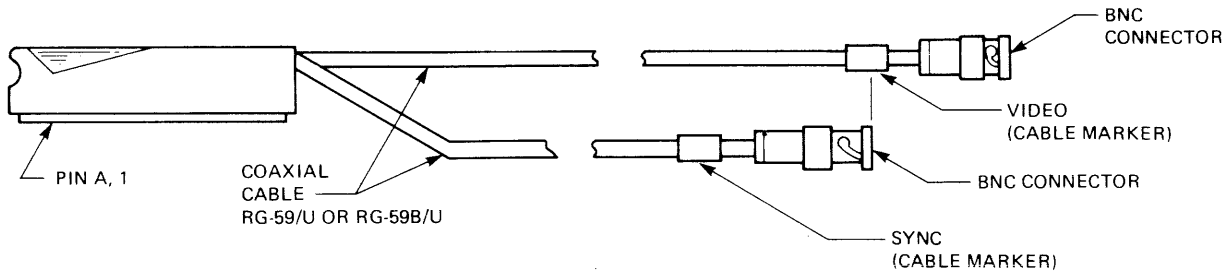
- e. Connectors for option 003 are prewired. The supplied cables are 7.5 meters (25 ft) in length. Fabricate extension cables if necessary.
- f. Check out any fabrication work and then install cards in appropriate slots of computer or I/O extender card cage. Use procedure given in paragraph 2-12, step g.
- g. Install TV interface cable 48-pin connectors on appropriate cards. Roll up and tie back or remove cables which are not used. Cabling is shown in figure 2-3.
- h. Connect the RED video connector from card A to the TV monitor RED video input connector. Similarly, connect the BLUE and GREEN connectors. Use coaxial adapter, part no. 1250-0071, if necessary.
- i. If the TV monitor requires external synchronization, connect the SYNC connector from card A to the TV monitor EXT SYNC connector.
- j. The only adjustment necessary for color operation is to ensure that the blanking level on all composite video outputs is the same.
- k. Using a multiple input oscilloscope display, display the pedestal of the three composite video signals. Connect the oscilloscope inputs to the composite video output (TP1) of each card (see figure 2-1).

- l. On card A (master card) adjust the blanking level to -1.0 volt with the pedestal control R5. Adjust the blanking levels of cards B and C to match the level set on card A, also with pedestal.
- m. Refer to the programming and operating manual for instructions on checkout in an RTE system (except RTE-B) for color operation using a color bar pattern. For off-line checkout and other operating systems, use the color bar pattern of the diagnostic program described in Section IV.

2-16. MULTI-LEVEL GRAY OPERATION

2-17. Two or three cards must be used in multi-level gray operation. Four or eight levels of gray can be produced by two or three cards, respectively. The cards must sit side by side in either the computer I/O card cage or I/O extender. The master card (designated as card A) must be placed in the highest numbered slot of the group and will be addressed by the select code (or LU number in RTE systems) assigned to the TV interface subsystem. The master card is followed in descending order by slave card B and slave card C. The card and cabling setup is shown in figure 2-3. Perform the following procedure to install multiple gray level cards:

- a. Review the black and white operation installation procedure given in paragraph 2-11. Observe the power supply and current requirements of the cards and other considerations such as I/O with DMA (or DCPC) and all cautions and notes.
- b. The wiring of three-card cables and the triple PC card connector for gray scale is shown in figure 2-4, using option 003. Two-card setups, using single hoods, should be wired according to figure 2-4 with card C deleted and the hoods assembled as shown in figure 2-2.
- c. Place a small piece of tape on each card and label them A (master), B (slave 1), and C (slave 2).
- d. Set jumpers on cards according to table 2-1 for scanning requirements and table 2-2 for multiple card operation.
- e. Connectors for option 003 are prewired. The supplied cables are 7.5 meters (25 ft) in length. Fabricate extension cables if necessary.
- f. Check out any fabrication work and then install cards in appropriate slots of computer card cage. Use procedure given in paragraph 2-12, step g.
- g. Install TV interface cable 48-pin connectors on appropriate cards. Roll up and tie back unused cables, or remove cables if their future use is unlikely. Cabling is shown in figure 2-3.
- h. Connect the composite VIDEO connector from card A to the TV monitor VIDEO IN connector. Use coaxial adapter, part no. 1250-0071, if necessary.



PARTS INCLUDED WITH CONNECTOR 02313-60010.

ITEM	DESCRIPTION	PART NO.
1	CONNECTOR HOOD	5040-6071
2	SELF-TAPPING SCREW	0624-0098
3	MOUNTING BLOCK	5040-6072
4	SELF-TAPPING SCREW	0624-0098
5	PAN-HEAD SCREW (4.40 x .562")	2200-0091
6	HEX NUT (4.40 x .187")	2260-0002
7	CONNECTOR, 48 PIN	1251-2518
8	CABLE CLAMP	5040-6004
9	SET SCREW	3030-0143

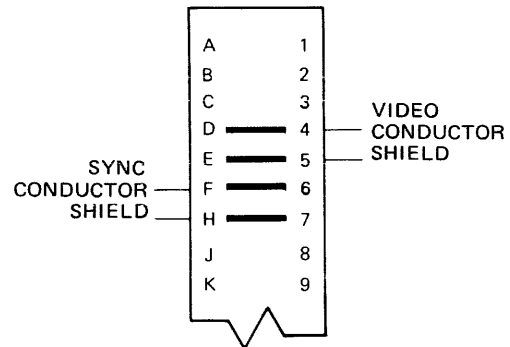


Figure 2-2. Cable Fabrication

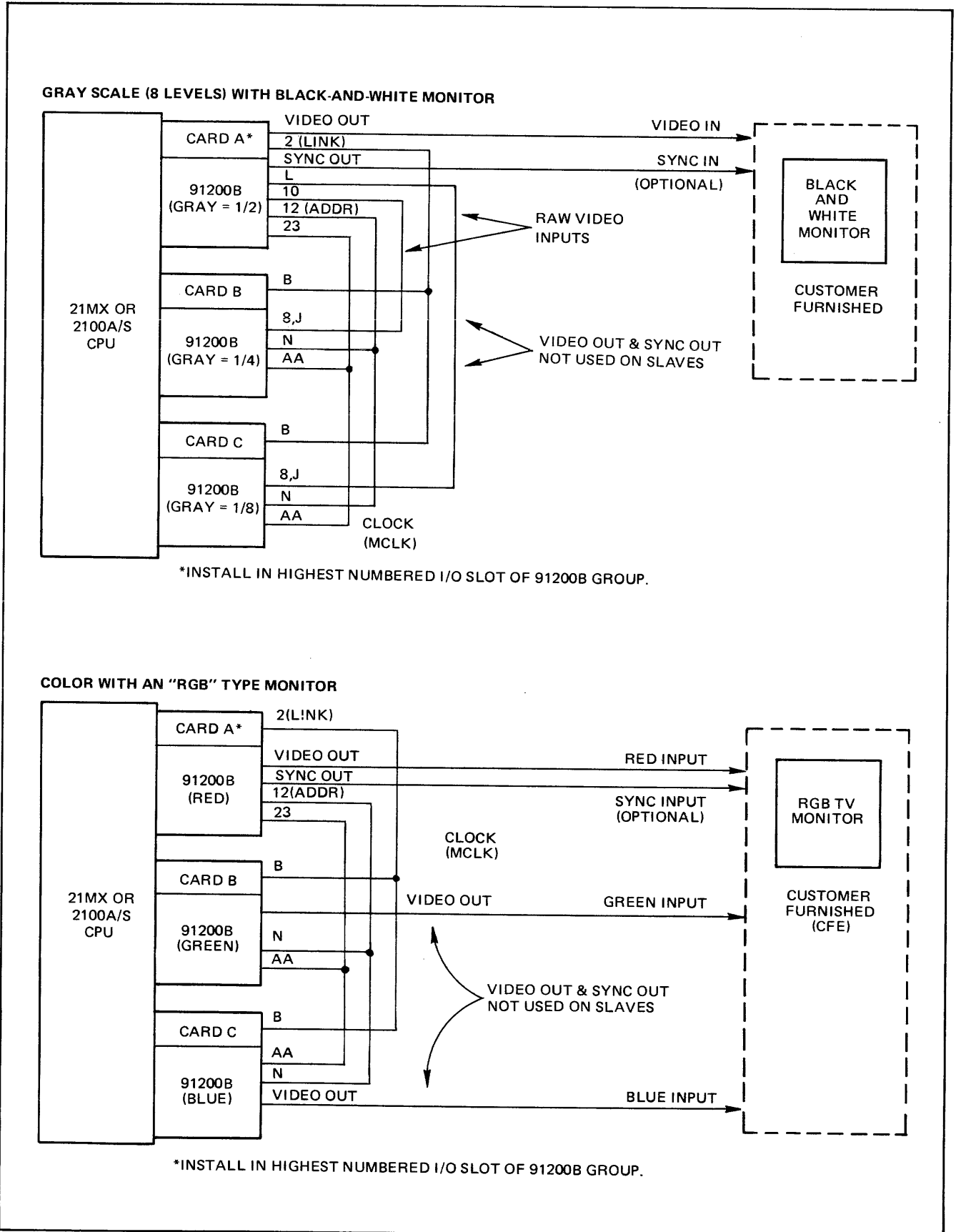


Figure 2-3. Multi-Level Gray and Color Installation Diagram

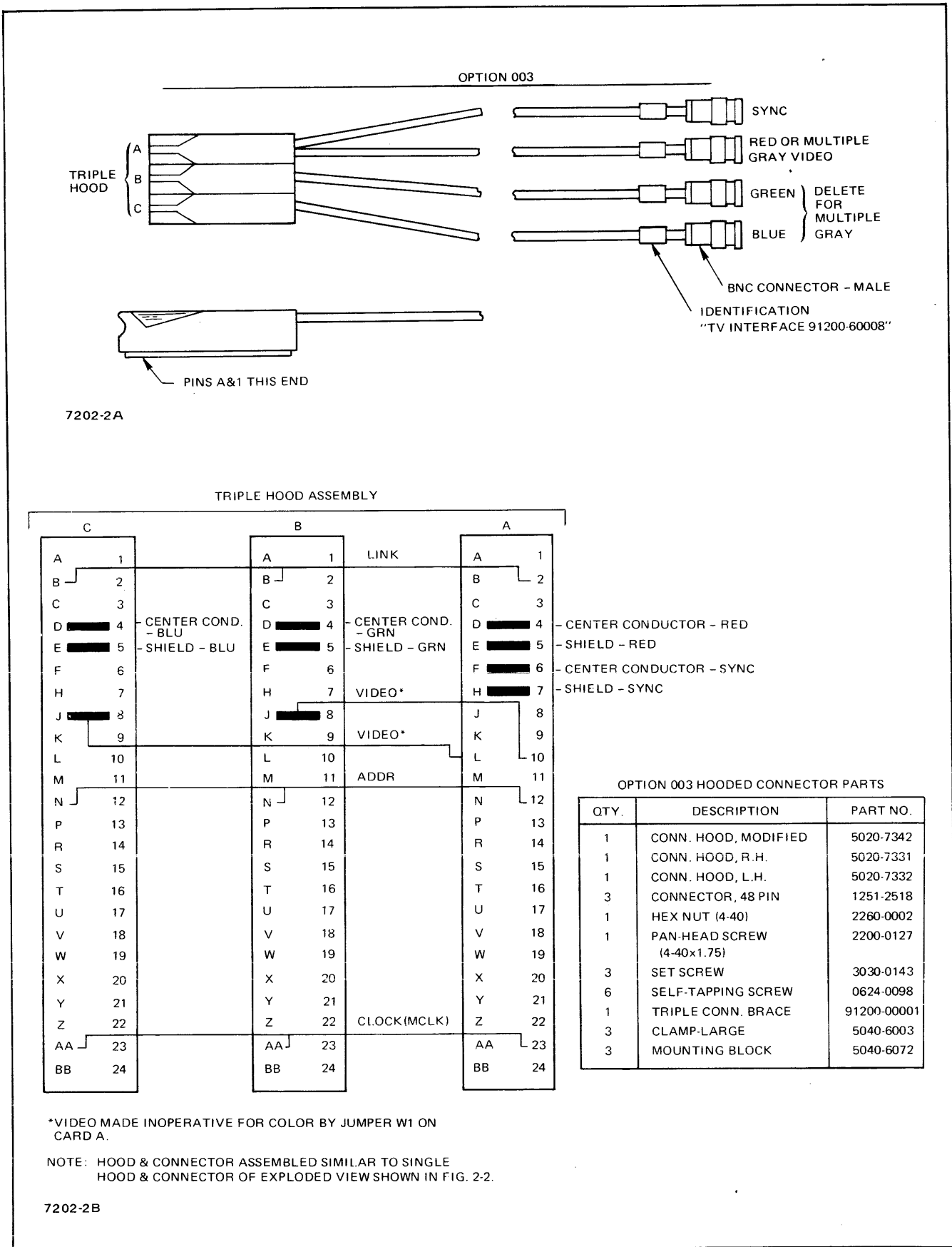


Figure 2-4. Triple-Hood Assembly for Color or Multi-Level Gray

- i. If the TV monitor requires external synchronization, connect the SYNC connector from card A to the TV monitor EXT SYNC connector.
- j. Connect an oscilloscope to card A (master) composite video output test point (see figure 2-1). Run verification or diagnostic program and display the color bar pattern. Adjust oscilloscope to display a staircase waveform between two sync pulses. The staircase waveform is shown in figure 2-5.

Note: There is an interaction between the three card A adjustment controls. Repositioning of one or more of these controls may be necessary.

- k. Use offset control R6 to position the top of the staircase at 0 volt. Set the blanking level at -1.0 volt using pedestal control R5. Use contrast control R7 to equalize each step in the staircase waveform. Refer to figure 2-1 for control location. An eight-level staircase waveform is shown in figure 2-5. With two cards, only steps 0,2,4, and 6 are present such that the white level is actually a 3/4 white.
- l. Refer to the programming and operating manual for instructions on checkout in a RTE system (except for RTE-B operating systems). For off-line checkout, the vertical bar pattern used in the diagnostic program described in Section IV may be used.

2-18. REMOTE TV MONITORS

2-19. One to five TV monitors, with parallel high impedance connectors, may be connected to one TV interface card. Refer to figure 2-6 for an example connection of TV monitors using the daisy chaining technique. The total permissible cable length is 500 meters (1640 ft). Refer to paragraphs 2-6 and 2-8 for monitor and cable requirements.

2-20. When operating in color applications, the connection of additional monitors is similar to figure 2-6. Each video cable is treated the same as the single video cable shown.

2-21. RESHIPMENT

2-22. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the interface card.

Note: Do not ship crystals with the TV interface card.

2-23. Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-24. If standard factory packaging material is unavailable, wrap the item in Air Cap TH-240 cushioning (or equivalent) manufactured by Sealed Air Corp. Hawthorne, N.J. and place in a corrugated carton (200 pounds test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful shipping.

Note: In any correspondence, identify the TV interface card by part number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

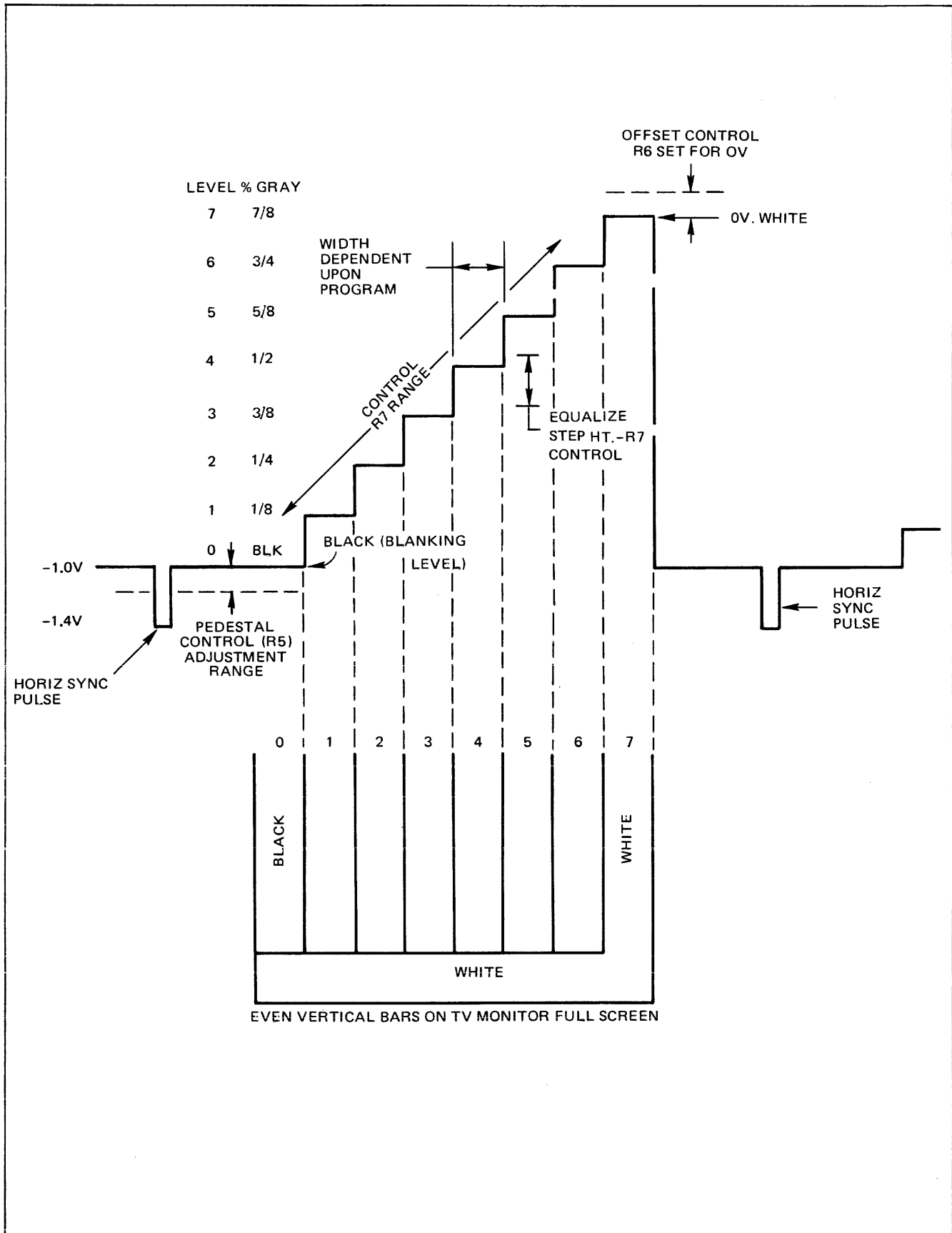


Figure 2-5. Multi-Level Gray Adjustment Waveform

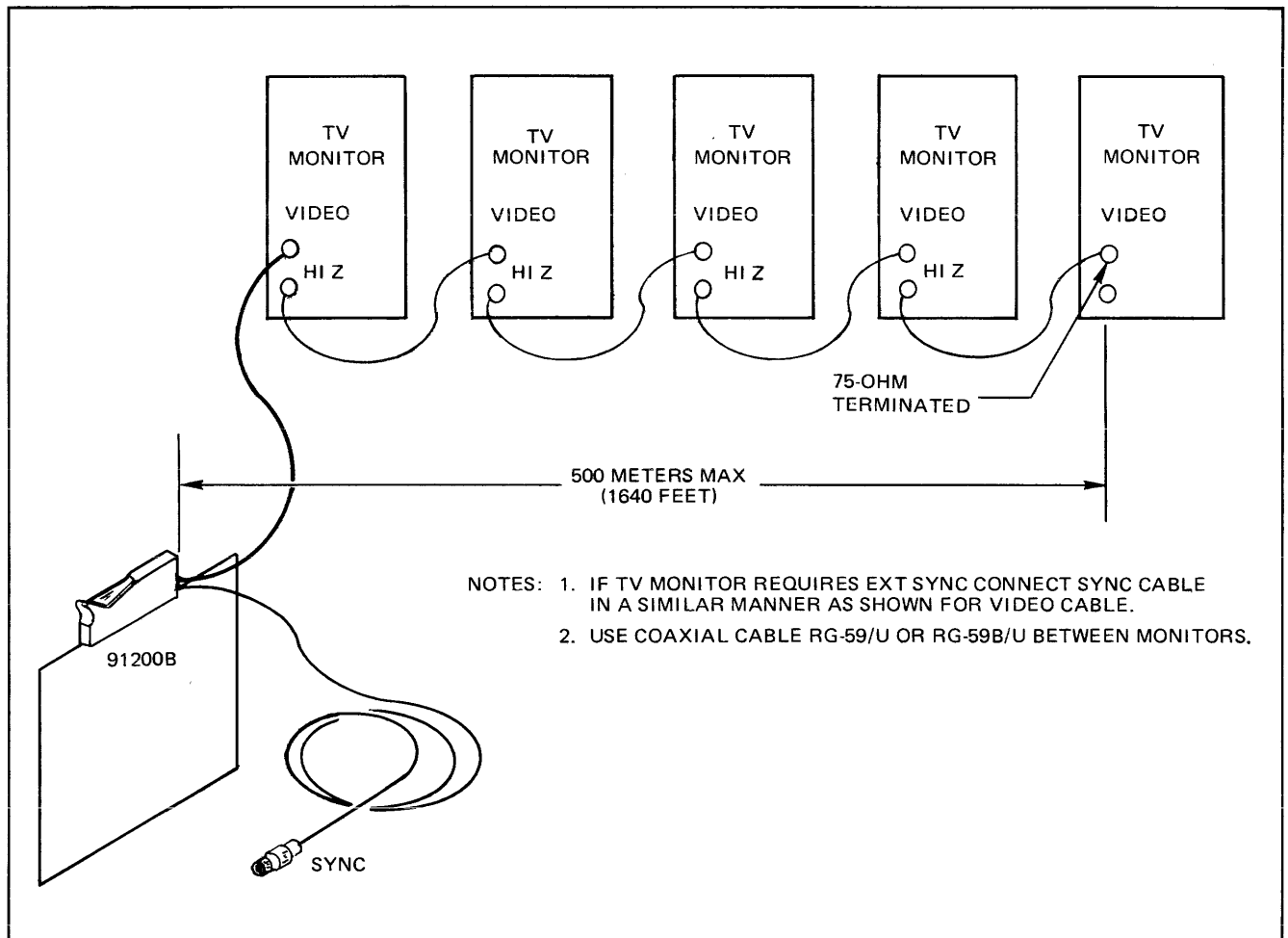


Figure 2-6. Multiple Monitor Connection Diagram

PRINCIPLES OF OPERATION

SECTION

III

3-1. INTRODUCTION

3-2. This section provides block diagram functional descriptions of the TV interface card.

3-3. GENERAL

3-4. Mnemonics are used to abbreviate signal names; e.g., NSTB (strobe) and NCLK (clock). The polarity convention used is that when a mnemonic beginning with the letter N is active, the logic level is low. Mnemonics for the same signals after logic inversion have the letter N removed. Thus, a strobe makes NSTB low and STB high. Similarly, a clock makes NCLK low and CLK high.

3-5. MODES OF OPERATION

3-6. The TV interface card is capable of three modes of operation to satisfy requirements for three different scanning rates. Operating modes are controlled by jumper placement and the selection of a crystal as specified in table 2-1. Mode I is the American Broadcast Standard, Mode II is the European Broadcast Standard, and Mode III is a non-standard scan to achieve full 256 vertical resolution with a 60 Hertz vertical scan rate. Table 3-1 lists the card and signal specifications for each mode. Figures 3-1 through 3-4 show idealized waveforms and relationships for each mode of operation.

3-7. VIDEO SIGNALS

3-8. There are 256 points of data and 64 clock counts for horizontal blanking on each video signal horizontal line. A clock count is defined as a clock pulse interval, shown as (T) in figure 3-1. Thus, each horizontal line has the equivalent of 320 clock counts, 256 for data and 64 for blanking. Figure 3-1 illustrates the typical video signal horizontal line for the TV interface card. Each data point in the video signal is clocked and displayed as a discrete dot if jumper W6 on the card is IN. Each data point will be unclocked, blending in with adjacent points to be displayed as a line, if jumper W6 is OUT. The video polarity can be programmed through the computer so that the data points can be written black-on-white or white-on-black.

3-9. Figures 3-2, 3-3, and 3-4 show the retrace portion of the video field for the three scan modes. The timing information for the included equalizing pulses, sync pulses, and intervals is given in table 3-1.

3-10. The vertical retrace interval is constructed through the use of groups of equalizing, horizontal, and vertical sync pulses. The duration of the vertical retrace interval is dependent on operating mode (I, II, or III). For example, in figure 3-2 showing the American Standard, the retrace interval from the end of the first field is 1.397 msec (22 horizontal line scans). In order to interlace the fields, the vertical retrace interval is extended an extra horizontal line scan, or 23h, after the second field. When used without interlace, all fields are the same as the first field with 22 horizontal line scans during vertical blanking (262 lines per field, 60 fields per second).

3-11. The TV interface card provides the option of blanking the second field through the use of jumper W11. Normally, both fields contain identical information with jumper W11 out. If the second field is blanked, it may be necessary to use a monitor with a long persistence phosphor screen CRT. The long persistence phosphor screen CRT's are generally green instead of white.

3-12. COMPUTER I/O SIGNALS

3-13. Since the TV interface kit is designed to be compatible with HP 2100A/S and HP 21MX Computers, reference should be made to the appropriate computer manual for a comprehensive discussion of I/O signals. A brief description of the computer I/O signals and their interaction with the TV interface card is given in Table 3-2. The 86-pin edge connector serves as the interface point between card and computer. Refer to figure 3-5, the functional diagram for the TV interface card, which identifies input and output signals and their pin numbers.

3-14. EXTERNAL I/O SIGNALS

3-15. The primary output from the TV interface card is the composite VIDEO signal for driving TV monitors. A SYNC signal is also available for TV monitors which require external synchronization. For color or gray-scale operation using multiple TV interface cards, the following signals are connected between the cards: MCLK, RVID, BIN, CIN, LINK, and ADDR. These signal connections are described under installation procedures in Section II. There is a CLK and RA0 through RA15 signals for user implementation of a light pen. The 48-pin edge connector serves as the interface point between the card and external devices (TV monitors and other interface cards). Refer to table 3-3 for a brief description of the external I/O signals and to figure 3-5 for the edge-connector pin location of these signals.

Table 3-1. Operating Mode Specifications

	MODE I	MODE II	MODE III	UNITS
Lines per Frame	525	625	288	—
Lines per Field	262.5	312.5	288	—
Fields per Frame	2	2	1	—
Fields per Second	60	50	60	—
Frames per Second	30	25	60	—
Interlace	2:1	2:1	None	—
Lines of data per Field	240	256	256	—
Horizontal Scan Rate	15750	15625	17281.25	Hz
f*	1.587	1.600	1.447	μsec
s*	4.762	4.800	4.340	μsec
b*	6.349	6.400	5.787	μsec
h*	63.492	64.000	57.866	μsec
e*	2.381	2.400	2.170	μsec
v*	26.984	27.200	24.593	μsec
T*	198.413	200.000	180.832	nsec
Point Rate	5.040	5.000	5.530	MHz
Crystal Osc. Freq.	10.080	10.000	11.060	MHz

*Refer to figures 3-1 through 3-4.

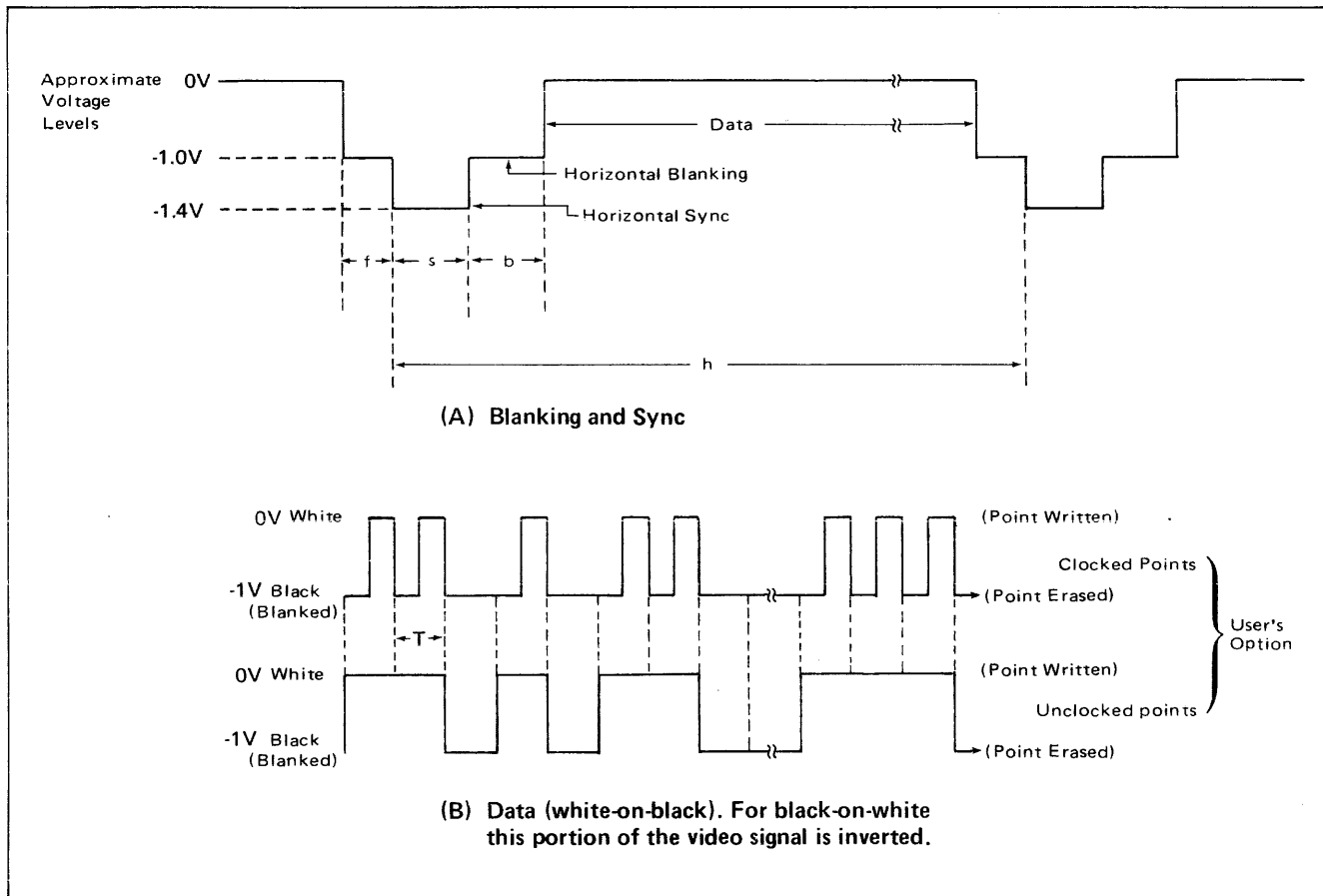


Figure 3-1. Video Signal, Horizontal Line Waveform

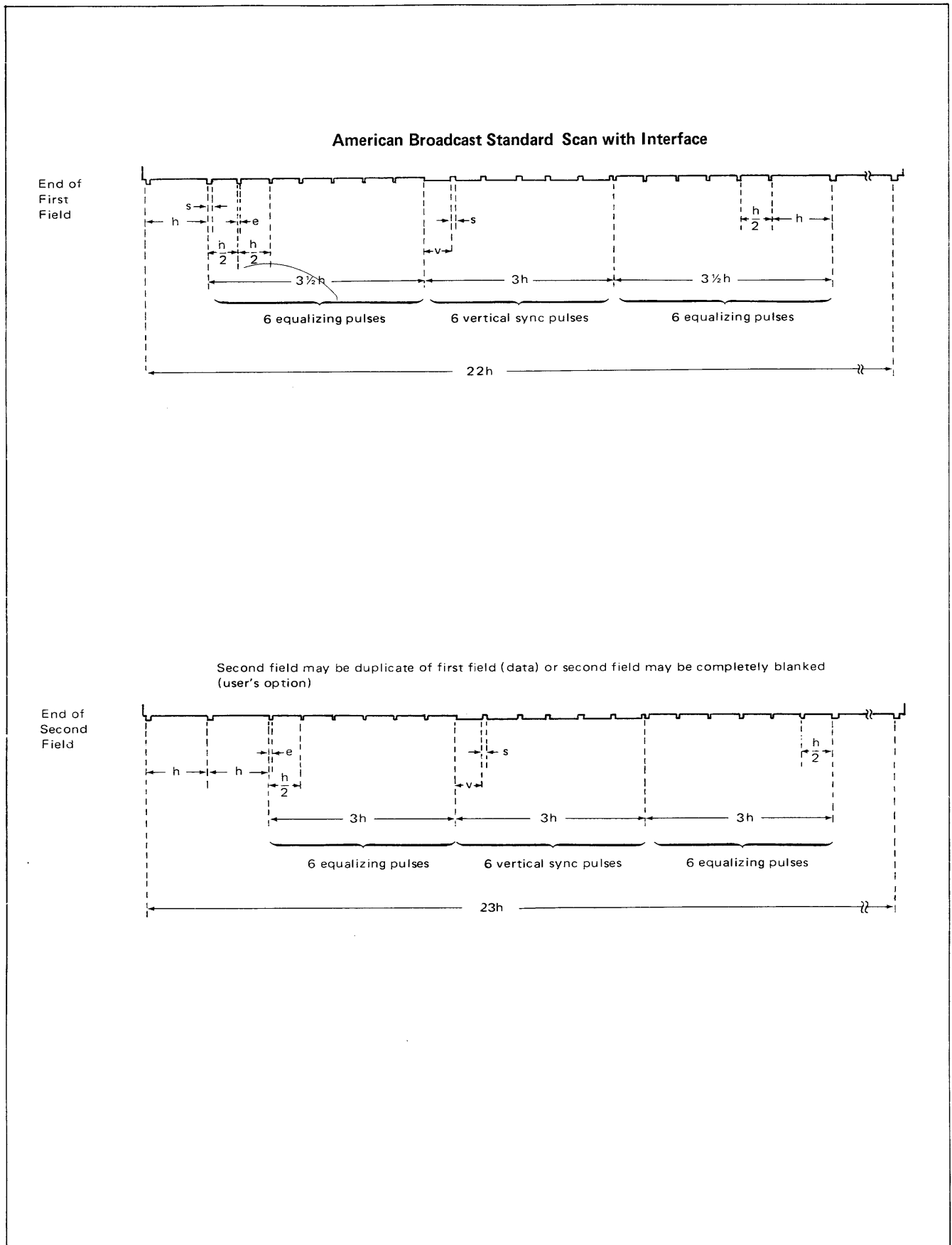


Figure 3-2. Video Signal, Vertical Retrace Waveform (Mode I)

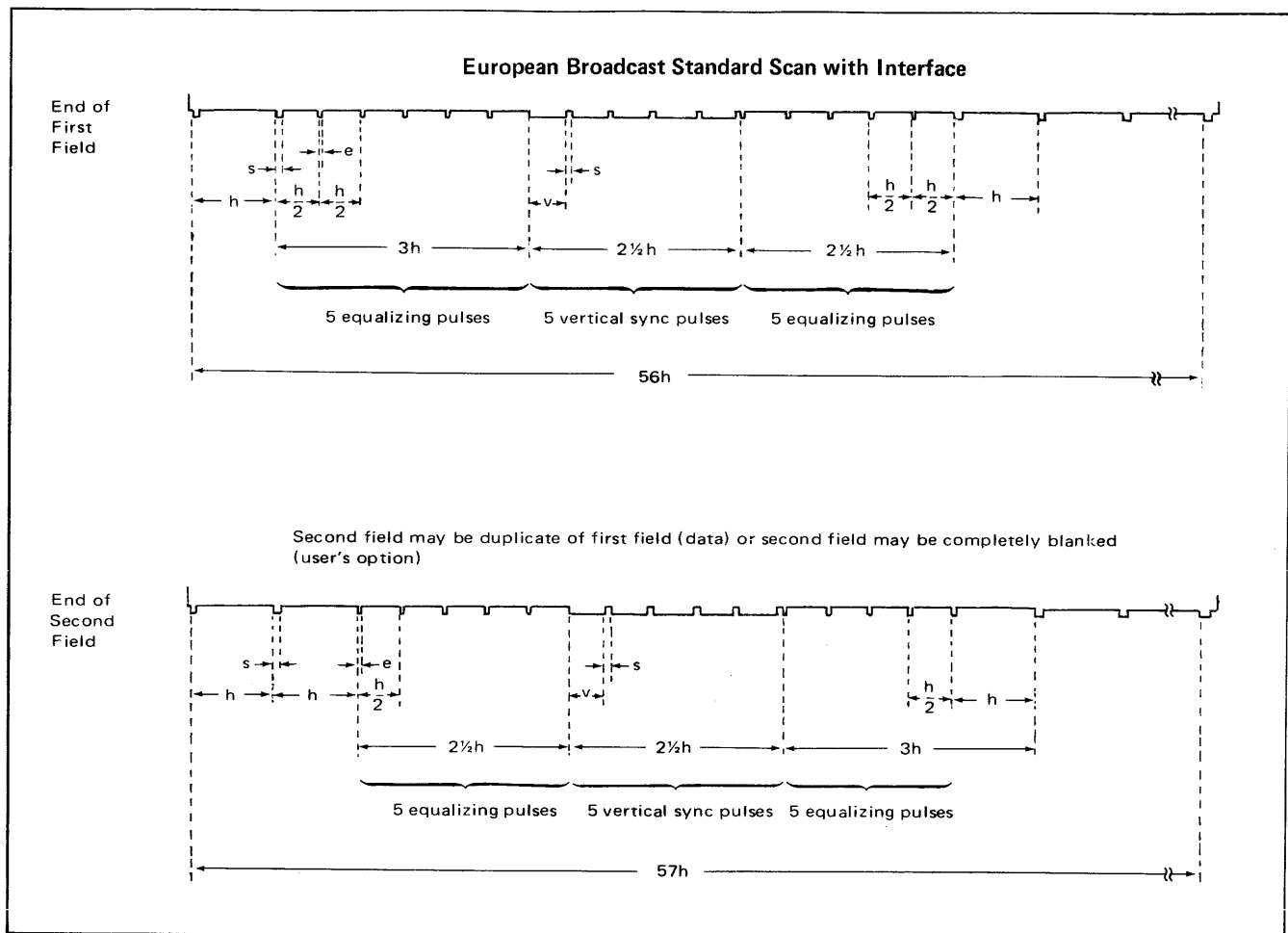


Figure 3-3. Video Signal, Vertical Retrace Waveform (Mode II)

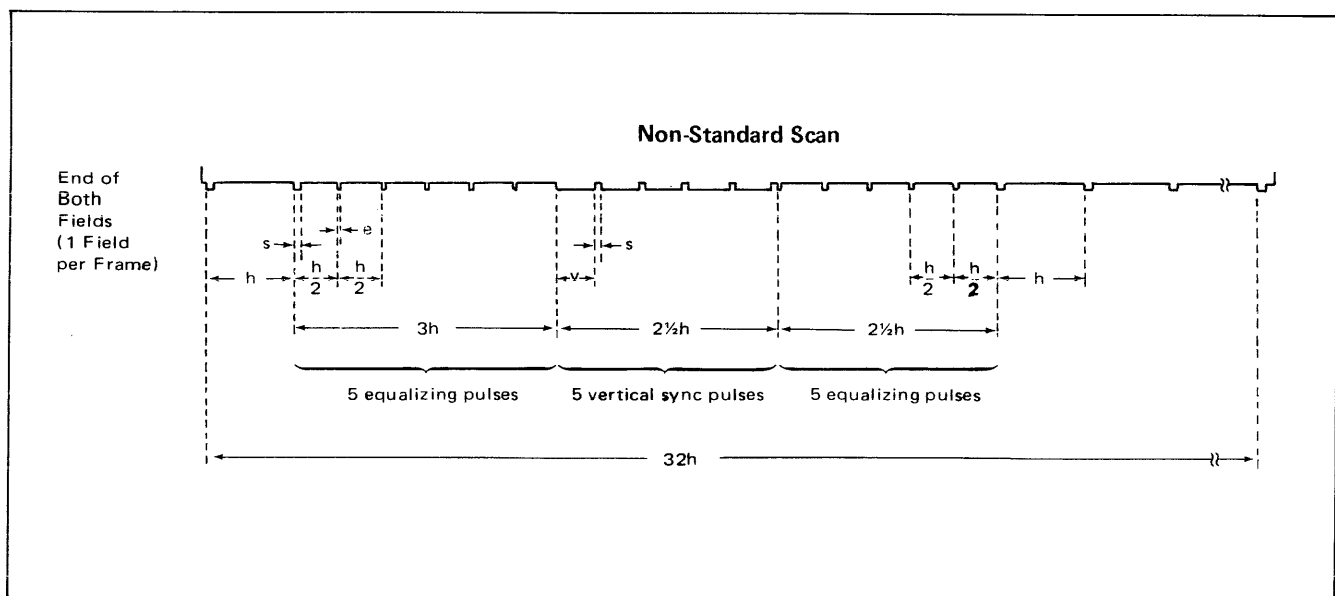
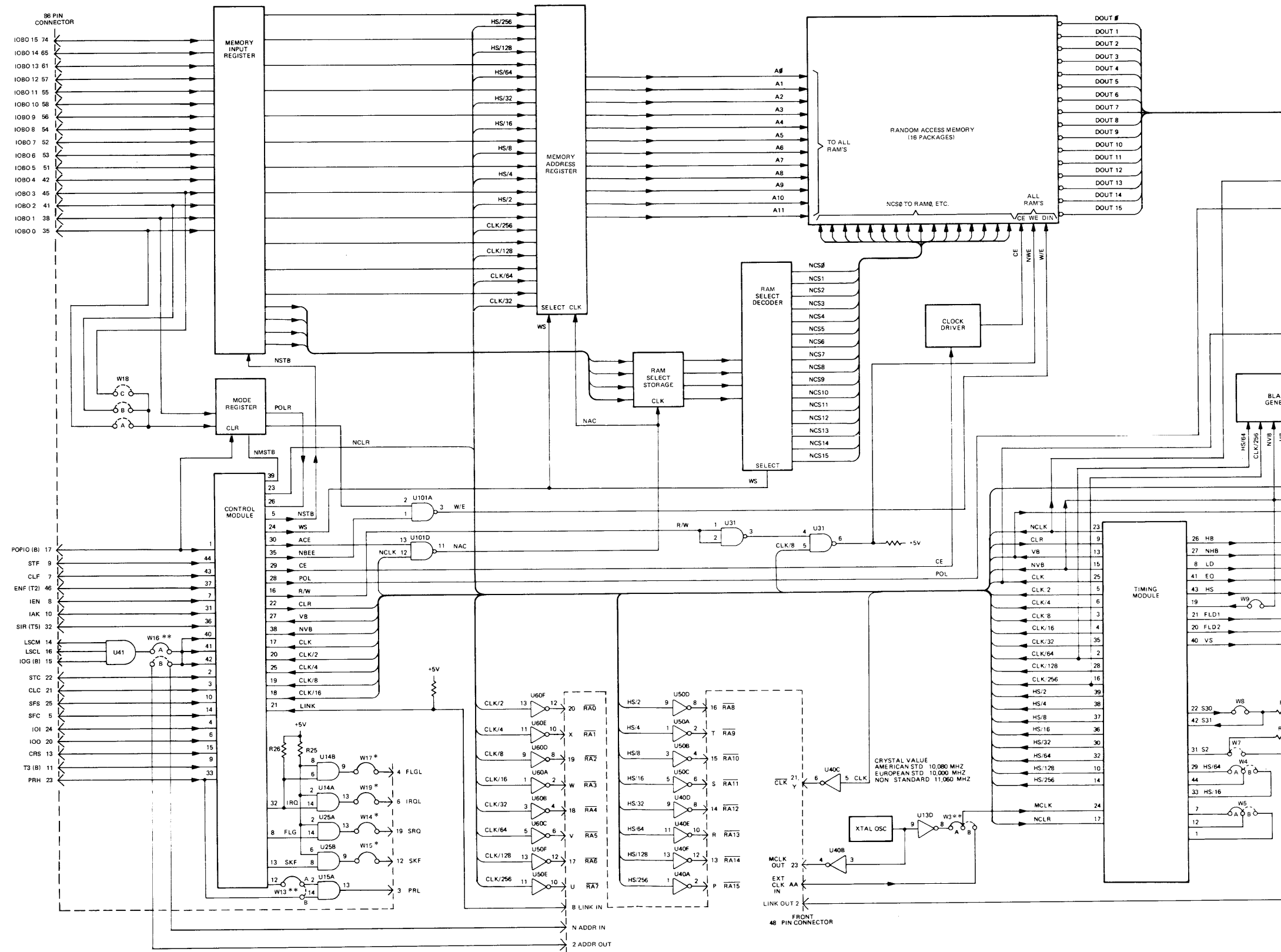


Figure 3-4. Video Signal, Vertical Retrace Waveform (Mode III)



* OUT FOR
** 8 FOR SLAVE

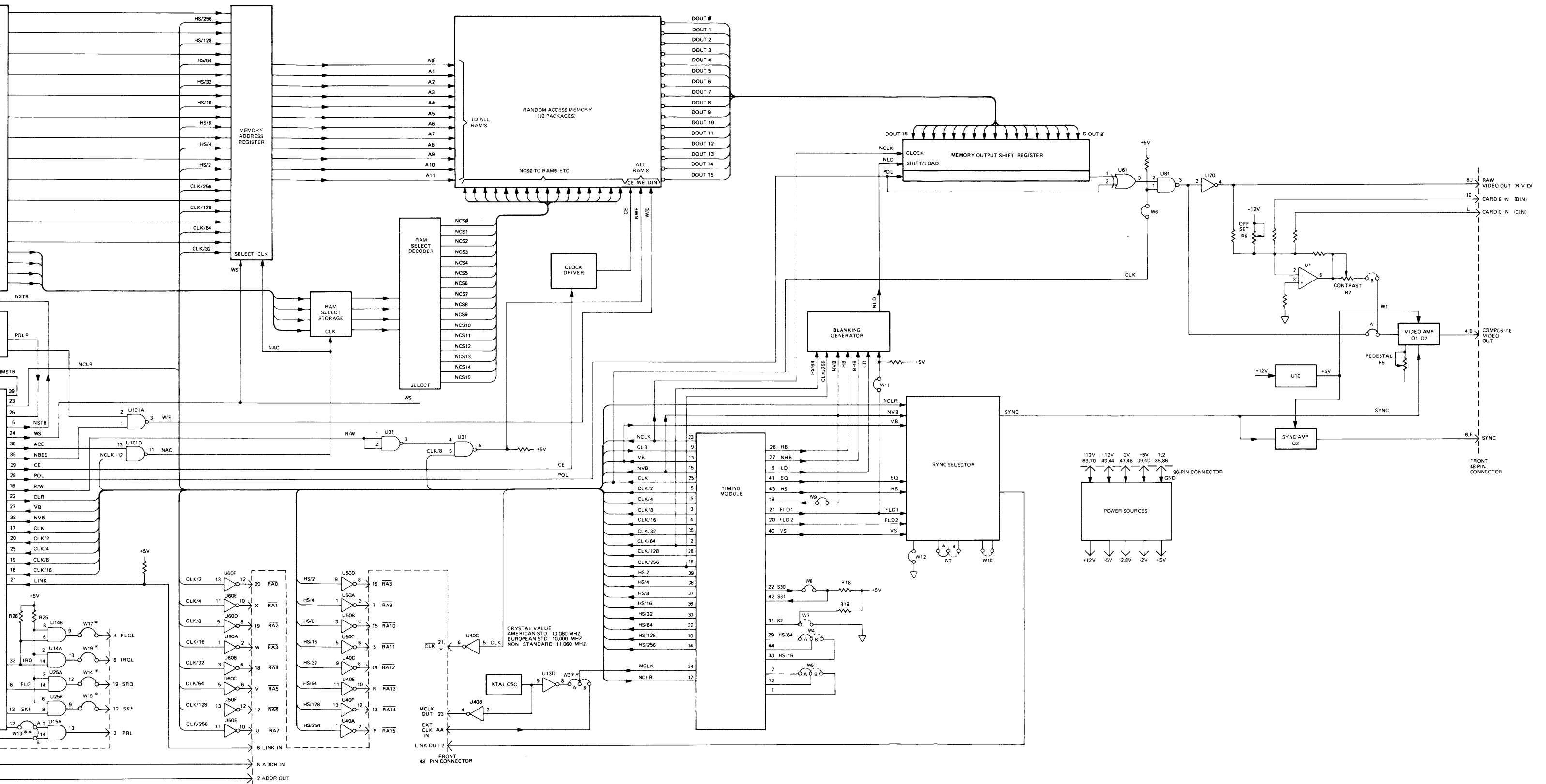


Figure 3-5. TV Interface Card, Functional Diagram

Table 3-2. Computer I/O Interface Signals

MNEMONIC	PIN	SIGNAL	DESCRIPTION
STC	22	Set control	Enables interrupt capability. Also initiates write or erase depending on the mode.
CLC	21	Clear control	Clears interrupt control upon execution of the CLC instruction. Sets mode control so that the next OTA will be interpreted as MODE information.
CRS	13	Control reset	Generated by EXTERNAL PRESET button on computer front panel or CLC 0 instruction or power on. Same effect as CLC signal. <i>Also, resets all counters in the timing module.</i>
ENF(T2)	46	Enable flag	Positive pulse at computer time T2. Sets flag if flag buffer is set.
IAK	10	Interrupt acknowledge	After detecting an interrupt, the computer responds with IAK which sets the interlock, causing the interrupt request to be cleared, preventing another interrupt from the same flag signal.
T3(B)	11	Computer time T3 (buffered)	Subcycle 3 of computer timing. Used to set flag buffer for MODE outputs.
SRQ	19	Service request	Output of flag used to initiate DMA (or DCPC) cycles.
IRQL FLGL	6 4	Lower select code Interrupt request and flag signals	IRQL and FLGL are signals used to initiate an interrupt.
PRH	23	Priority high	When high, indicates that no device of higher priority is requesting an interrupt. If low it prevents this card from interrupting. The interrupt is saved until PRH goes high.
PRL	3	Priority low	When low, prevents any interface card of lower priority from interrupting computer program. Will be low whenever processing an interrupt on this card or higher priority card.
LSCM	14	Lower select code most significant digit	The LSCM, LSCL, and IOG(B) signal combination determines the computer I/O slot to which the instruction portion of the computer I/O command word is directed. When the TV interface card is selected, all three signals will be high. Generates ADDR signal on card.
LSCL	16	Lower select code least significant digit	
IOG(B)	15	I/O group instruction	
IOBO0 thru IOBO15	35,38,41,45, 42,51,53,52, 54,56,58,55, 57,61,65,74	16-bit data word	16-bit parallel binary data word being output from computer to TV interface card.

Table 3-2. Computer I/O Interface Signals (Continued)

MNEMONIC	PIN	SIGNAL	DESCRIPTION
SIR(T5)	32	Set interrupt request	Positive pulse that occurs at computer time T5. If other prerequisites are met, sets interrupt request if flag is set or clears interrupt request following an IAK.
STF	9	Set flag	Sets interface card flag high.
IOO	20	I/O output operation	Strobes computer data word into interface card on OTA/OTB.
IOI	24	I/O input operation	Input strobe from LIA/LIB. Initiates bulk erase.
CLF	7	Clear flag	Clears flag and interlock. Also allows mode control to be cleared by T3(B).
SFS	25	Skip if flag set	Used to determine if flag is set. Causes SKF if flag is set.
SFC	5	Skip if flag clear	Used to determine if flag is clear. Causes SKF if flag is clear.
SKF	12	Skip flag	If issued it will cause program to skip an instruction. See SFS and SFC above.
IEN	8	Interrupt enable	High when the computer interrupt system is on, low when it is off. Must be high if an interrupt is to occur.
POPIO(B)	17	Power-on preset	Initialization command which presets interface card to known starting condition when power is applied to computer. Also issued by PRESET button. Causes bulk erase. Also see CRS.

3-16. FUNCTIONAL BLOCK DESCRIPTION

3-17. CONTROL SECTION

3-18. Refer to figure 3-5, functional block diagram, throughout the following description. The control section is contained in a single IC package called the Control Module. Within it are the standard flag and interrupt circuitry used in HP 2100-Series Computer interfaces, and the memory control functions. The control signals set up the card for memory read or write operations. During an I/O operation, an *interrupt acknowledge* sets a flag interlock flip-flop which inhibits further interrupt requests. A clear flag (CLF) must be programmed and issued by the computer to re-enable the interrupt circuit. (Most HP 2100-Series Computer interface cards do not include the flag interlock feature.) A CRS command from the computer resulting from a CLC0 program mnemonic (or computer front panel EXT PRESET, or LINK from the Master

Card to a Slave Card) will generate a clear (CLR) signal on the card and its opposite polarity NCLR signal. These signals reset the timing module and sync selector.

3-19. When either (CLC SC) or (CLC 0) occurs the control module is set so that the next OTA will be interpreted as mode information. The least significant bits (IOBO 0 through IOBO 3, depending on jumper W18 settings) of the next word are strobed into the mode register by the mode strobe (NMSTB) signal. IOO initiates NMSTB and NSTB signals. Normally, mode bit 1 is zero (white-on-black on BW monitors) unless polarity reversal has been programmed (POL high). The mode signals for color are given in table 3-4. Bulk erase is caused by either POPIO (power-on preset) or IOI from program LIA, MIA, etc. POPIO also sets CRS high which resets the counters. Bulk erase is initiated by NBEE (low) from the control module at input 1 of U101A forcing W/E high at the input D_{1N} of the RAM's, which is the erase condition.

Table 3-3. External I/O Signals

MNEMONIC	PIN	SIGNAL	DESCRIPTION
LINK OUT	2	Multi-card Synchronization (Master Card)	When connected to LINK IN, resets counters and registers.
LINK IN	B	Multi-card Synchronization (Slave Card)	Receives LINK OUT from master card for frame sync.
VIDEO	4, D	Composite Video Output	Video signal with sync pulses to drive TV monitors through 75-ohm coaxial cable.
SYNC	6, F	Sync Output	Synchronization pulse train only. This is an auxiliary output for TV monitors requiring external sync.
RVID	8, J	Raw Video Output (Slave Card)	Video without sync, connects to BIN or CIN of master card for multi-level gray operation (TTL level).
BIN	10	Card B Input (Master Card)	Raw video input signal from slave card B for multi-level gray operation.
CIN	L	Card C Input (Master Card)	Raw video input signal from slave card C for multi-level gray operation.
ADDR OUT	12	Select Code Addressed (Master Card)	Indicates master card addressed by computer.
ADDR IN	N	Input for Addressed Encode (Slave Card)	Slave card input for addressed signal. Enabled by jumper W16 in position B.
RA0 thru RA15	13-20 and P-X	Read Address	A 16-bit word (ground true) indicating the read address of the point being displayed. Current point read address bits are auxiliary output for user implementation of a light pen.
CLK OUT	21, Y	Clock	Point clock to aid in light pen implementation.
MCLK OUT	23	Master Clock Output	Clock signal for locking multiple cards together for color or multi-level gray operation.
EXT MCLK IN	AA	External Master Clock Input	Card can operate from an external clock when this signal is present and jumper W3 is in position B. For slave cards.

3-20. The mode bit 1 gives normal polarity of the video when logic 0 (low) and the inverse polarity when logic 1 (high) which gives the complements of the colors. Mode bit 1 exits the mode register as the polarity reference (POLR) signal to a polarity flip-flop in the control module. The POLR signal is gated through by the vertical blanking (VB) signal to enable the polarity signal (POL) which goes to the shift register. Therefore, signal polarity can only be changed at the end of a field during the blanking period.

3-21. The clock timing signals (CLK, CLK/2, CLK/4, CLK/8, CLK/16) are used to generate the following: read/write (R/W), word select (WS), chip enable (CE), and address clock enable (ACE). WS is the same as R/W inverted as long as bulk erase is not in effect. The R/W signal is routed through two "nand" gates for pulse shap-

ing and becomes the write enable signal (NWE) which goes to the WE terminal on all 16 RAM's. A low (logic 0) NWE signal selects the write mode. All memory read/write functions take place when the clock signal CE, through the clock driver, is high. The ACE can only occur when the RAM's are not clocked (absence of CE). ACE gates NCLK through U101D producing the address clock signal (NAC) for the RAM address storage and memory address register. This ensures that the address lines to memory are settled before a pulse arrives on the CE line.

3-22. Multiple cards for color or gray scale are addressed simultaneously by LSCM, LSCL, and IOG(B) generating ADDR through U41 as though they were located in the one computer select code position of the master card. The parallel addressing comes from the positioning of jumper

W16 at "A" for the master and "B" for the slaves. This sends the ADDR OUT signal through the 48-pin connector to ADDR IN on the slaves. IOO initiates NMSTB and/or NSTB to strobe the TV interface card(s). Mode bit 0 on each card is selected by jumper W18 which applies IOBO 0 to master card A, IOBO 2 to slave card B and IOBO 3 to slave card C. Thus, the mode programming word, according to the three-bit combinations listed in table 3-4, will provide a color display or gray scale.

Table 3-4. Multiple-Card Mode Word Signals

IOBO BITS 3-2-0	3-CARD COLOR	3-CARD BW	2-CARD COLOR	2-CARD BW
0-0-0	white	7/8 wh	yellow	3/4 wh
0-0-1	cyan	3/8	green	1/4
0-1-0	magenta	5/8	red	1/2
0-1-1	blue	1/8	black	black
1-0-0	yellow	3/4	yellow	3/4 wh
1-0-1	green	1/4	green	1/4
1-1-0	red	1/2	red	1/2
1-1-1	black	black	black	black

Note: IOBO 1 is 0 (low) for the above. Programming IOBO 1 as 1 (high) reverses the video polarity. This reverses black and white on BW monitors and gives complementary pairs on color monitors as follows: three card colors are white - black, red - cyan, green - magenta, blue - yellow; two card colors are yellow - black, red - green.

3-23. TIMING SECTION

3-24. The timing section consists of the crystal oscillator, the timing module, the sync selector, and the blanking generator.

3-25. The repetition rate of the master clock signal is dependent on the selected oscillator crystal. During color or multiple level gray operation, two or three TV interface cards (designated as cards A, B, and C) may be employed. On master card A, jumper W3 is placed in position A for the clock signal MCLK to be applied to the timing module. Jumper W3 on slave cards B and C is set to position B so the clock signal comes from EXT CLK IN. In this manner all cards are clocked by one master clock (MCLK) signal, thus ensuring synchronization of all cards as a group.

3-26. Slave card operation requires a LINK signal into the control module from the master card to maintain sync between cards. The link signal comes from the sync generator during the vertical blanking period of field one when all counters pass through zero. This ensures that the master and slave cards are synchronized.

3-27. The MCLK signal is routed to the timing module where it is divided by two to produce the basic clock pulse (CLK,NCLK) which is the point time used to shift the registers, control basic card timing, clock the discrete display points, etc. An 8-bit horizontal point counter divides

the basic clock pulse to produce the CLK/2, CLK/4, CLK/8, CLK/16, CLK/32, CLK/64, CLK/128, and CLK/256 clock pulses. The total of 256 is normal for one horizontal line of the visible display. Upon entering horizontal blanking, the counter counts to 64. The counter resets and begins counting for the next visible line to repeat the count of 256. The value of the 8-bit horizontal point counter during the visible portion of the horizontal line provides the displayed point horizontal address for the memory section. The total count cycle is 320 counts providing in addition to the 256 point line, one horizontal (HS) sync pulse, two equalizing (EQ) pulses, two vertical sync (VS) pulses and the horizontal blanking (HB) pulse.

3-28. An 8-bit vertical line counter divides the horizontal sync pulses by 240 or 256, according to the scan mode settings of jumpers W5 and W7. At the last count, the timer switches from line scan to the vertical blanking period, applying blanking VB and counting a predetermined number of counts based on the mode of operation selected by jumpers W4 and W8. At the end of the blanking count, the counter resets VB. The vertical line counter provides the timing pulses HS/2, HS/4, HS/8, HS/16, HS/32, HS/64, HS/128, HS/256. Each time the vertical blanking period is started or stopped, a flip-flop is toggled to produce the field signals FLD1 and FLD2 when the jumper W9 is set for interlace in the American or European scan modes.

3-29. The clear (CLR, NCLR) inputs from the control module serve to reset all counters, flip-flops, and registers. Refer back to table 2-1 for the effect of jumpers on the scan parameters.

3-30. The sync selector operates only during vertical blanking. A 5-bit counter, when enabled during the vertical blanking period, counts the vertical sync (VS) pulses. When not in the vertical blanking period (display visible), the vertical blanking (VB) signal holds the entire counter in the zero state. During this time VB is low and the ground-true vertical blanking NVB signal is high.

3-31. Jumpers W2, W10, and W12 are employed to reset the counter after counting the appropriate number of VS pulses for the operating mode. W10 provides vertical sync (VS) reset for Modes II and III, W12 provides counter reset for Mode I, and W2 establishes the number of equalizing pulses for the mode selected.

3-32. MEMORY SECTION

3-33. The TV interface card contains a 65,536-bit solid-state memory made up of sixteen 4096-bit random-access memory packages (RAM's). The bits in the memory are directly related to the points displayed on the TV monitor in a 256-by-256 point array. One 16-bit computer word is used to address any point in memory with the lower 8-bit byte addressing the X (horizontal) axis of 256 (0-255) locations, and the upper 8-bit byte addressing the Y (vertical) axis of the 256 (0-255) locations.

3-34. The input 16-bit computer word (IOBO 0 through IOBO 15) contains the address of the particular point in memory which is to be written or erased. The control signal NSTB strobes the memory input register and at NAC the computer word goes into the memory input register. The four least significant bits go into the RAM select storage. At the appropriate time, the word select (WS) signal goes high which enables the RAM select decoder to select a RAM. At the same time, the upper twelve bits are stored in the memory address register.

3-35. The 12 address lines from the memory address register are common to all 16 RAM's. Within each RAM package there is a 64-by-64 array (4,096 points). The lower six address lines (A0 through A5) are used for row selection and the upper six address lines (A6 through A11) are used for column selection. The output of the RAM select decoder (which is a pair of 256-bit read only memories) will select only one RAM package. This pre-programmed ROM applies the chip select (NCS) signal to the addressed RAM.

3-36. The previously issued control word with mode information will determine whether a write or erase operation is to take place. NWE becomes low for write enable or high for read enable according to the gating (by U31) of the R/W signal from the control module and the CLK/8 signal from the timing module. The write/erase (W/E) signal is applied to all 16 RAM data input terminals. A logic low writes the point and a logic high erases the point.

3-37. On the selected RAM, the select terminal receiving the NCS signal effects the data-in, data-out, and write enable inputs. An NCS low enables data-in and data-out terminals to perform read/write operations. The NCS input must be low and all address lines must be stabilized on or before the rising edge of the clock CE signal. All read/write operations take place when the clock CE input is high. When the clock CE line is low, no operation can take place.

3-38. Refresh of the RAM's takes place more than ten times every two milliseconds by reading through the 64 row addresses of each of the 16 RAM's. The refresh takes place by reading in the following manner: When the WS signal high is present, the timing signals from the timing module (HS and CLK) are stored in the memory address register. WS also holds the select decoder in a pre-programmed state where all NCS lines are low to select all 16 RAM's simultaneously. Upon application of the NAC signal to the clock input of the memory address register, the timing signals are transferred onto the address lines. The read cycle continues when the CE input goes high on all RAM's.

3-39. The memory output 16-bit shift register operates with parallel input from the RAM's and serial shift output to U61 to provide the video output bit stream for each point of the video display in sixteen 16-bit increments for each 256 point line. The state of the NLD signal, applied to the shift/load input, establishes the input or output mode. When NLD goes low, parallel loading of DOUT 0 through DOUT 15 from the addressed RAM occurs on the next

NCLK clock pulse. Bit DOUT 0 is immediately available to U61. When NLD goes high, serial shifting of the data into U61 occurs with each NCLK clock pulse starting with DOUT 1. The polarity signal (POL) shifts in, replacing the data bits shifting out to fill the register.

3-40. When the 16th NCLK pulse after NLD high occurs, NLD goes low again which will load a second set of 16-bits from the addressed RAM. DOUT 0 of the second data word becomes immediately available to U61 followed by NLD high and NCLK to shift DOUT 1 to the output position, etc. Starting at the beginning of a horizontal line, after 16 parallel loads and shifts a total of 256 points have been output. Then NLD remains high so no more loading occurs, NCLK continues and the shift register output bits resulting from POL are applied to U61 pin 1 for blanking. The horizontal blanking period continues as long as NLD is high, lasting for 64 clock pulses. NLD then goes low to repeat loading data for the next line.

3-41. VIDEO SECTION

3-42. During the blanking period, the output (pin 3) of exclusive "or" gate U61 will be low. This is because POL, direct and through the register, is applied to the gate's two inputs (when both inputs of an exclusive "or" are the same, the output is low). The level is inverted in U81 "nand" gate to apply a high level to the video amplifier. A high level at this point results in a black (or blanked) level in the display.

3-43. The blanking activity described above for the horizontal line is repeated for the vertical period after the bottom line has been displayed. The blanking period for vertical retrace is determined by the operating mode (I, II, or III). The blanking generator inhibits NLD (ground-true signal) to provide a high whenever either vertical (NVB), horizontal blanking (HB, NHB), or FLD1 through jumper W11 occurs. The load signal (LD), the source of NLD, appears once every 16 clock pulses at the blanking generator input. The CLK/64 and CLK/256 timing signals function as control in selecting the blanking period, being "and" gated with the horizontal blanking signals HB and NHB. Normally, jumper W11 is absent and therefore field one input is always high. Installation of jumper W11 inhibits the second field in the interlace mode to accentuate discrete points in the Y axis. (Information in only one field is displayed.) In this case, the TV monitor should have a long persistence phosphor screen CRT to reduce screen flicker. When FLD1 goes low coincident with the second field, the output NLD signal is inhibited (signal is high) and provides blanking for the entire second field as explained in paragraph 3-40.

3-44. U81 clocks each display bit as long as jumper W6 is installed. When W6 is removed, the pull-up resistor on pin 1 holds the gate continuously open so that the discrete data points in memory merge together as lines (refer to figure 3-1B showing clocked and unclocked waveforms).

3-45. Polarity inversion of the video display is controlled in U61 in the following manner. When the polarity line POL is low and the display bit is high, the output of U61 is high resulting in white (or color) which is the normal convention. If POL is programmed high, then when the display bit is also high, the result is a low output for black. Therefore, programming POL from the normal low to high inverts the video display from white-on-black to black-on-white (or color complements in color displays).

3-46. The video circuitry includes three transistors (Q1, Q2, and Q3), an inverter (U70), and operational amplifier (U1) and 5 volt regulator U10. The output from "nand" gate U81 is the raw video routed to inverter U70 then to the operational amplifier U1 for multiple gray-scale operation or routed through jumper W1-A to video amplifier Q1 for single BW or color operation.

3-47. During black-and-white or color operation jumper W1-A is installed. Raw video is applied to Q1 and

the sync signal is applied to Q2. The collectors of transistors Q1 and Q2 are tied together to provide the output composite video signal with sync. The composite video output has a 75-ohms source impedance to drive 75-ohm coaxial cable with the video levels of white at 0 volt, black at -1 volt, and sync at -1.4 volts. The sync output from Q3 is a 4.0-volt (nominal) negative-going pulse.

3-48. In multi-level gray or color operation, two or three TV interface cards may be used. Refer to Section II for card configuration information. One card is designated the master (card A) and the others are slaves (cards B and C). During multi-level gray operation, the raw video signals from all the cards are summed at the input of the operational amplifier (U1) on the master card to produce a single video signal going to Q1 through jumper W1-B. Sync is added by Q2 as in single card operation. Three controls (R5, R6, and R7) allow minor level adjustments (refer to figure 2-5).

4-1. INTRODUCTION

4-2. This section describes a diagnostic test procedure which checks the TV interface card for proper operation. The description of the test procedure is supported by example test patterns.

4-3. EQUIPMENT REQUIRED FOR TEST

4-4. The following items are required to run a diagnostic test of the TV interface card:*

- a. An HP 2100A/S or HP 21MX Computer.
- b. The diagnostic paper tape, part no. 91200-16003, furnished as part of the kit.
- c. An input device to enter the program into memory (e.g., an HP 2748B Tape Reader) with its interface card and cable.
- d. The TV monitor interconnecting cable, part no. 91200-60006, or multiple-card cable assembly, part no. 91200-60008, or user fabricated cables according to figures 2-2 and 2-4.
- e. User supplied TV monitor.

4-5. DIAGNOSTIC TEST PROCEDURE

4-6. The diagnostic program consists of a go no-go test, a super test for examination of individual patterns, a RAM test, and a color bar or gray-level bar test pattern. The test results appear on the display register of the computer and the test patterns are shown on the TV monitor.

4-7. The purpose of the diagnostic is to allow the operator to do the following:

- a. Check the TV interface card for proper operation.
- b. Check and adjust the TV monitor horizontal and vertical gain and positioning.
- c. Check and adjust the TV monitor focus.
- d. Check and adjust the TV monitor for pin cushion distortion and linearity.
- e. For multiple card installations, adjust gray scale or color.

*Next lower priority (higher numbered) I/O slot must have an interrupt type I/O card installed in it or an "error 7" will occur.

- f. Check the TV interface card for missing storage bits.
- g. Check the erase time using a 44 ms software timer.

4-8. TEST PROGRAM CONFIGURATION

4-9. The following procedure assumes the programmer/operator is familiar with the operation of his computer. The diagnostic is an absolute program that can be loaded into the computer at any time, off-line from the main operating system. The procedure is as follows:

- a. Examine the TV interface card jumpers to be certain of the scan mode of operation.
- b. Be sure that the TV interface card (or cards) is installed in the computer I/O slot in the proper order. The proper order is determined by the required I/O slot order of the system in which it is being used. Ensure that the card is seated firmly, and see that the video cable is connected to the TV monitor. (Installation of the TV interface card must follow the rules for I/O card installation in HP 2100-Series Computers. Refer to the appropriate manuals as required.)
- c. Refer to the applicable procedure in paragraph 4-31 or 4-34, respectively, for basic binary loader (BBL) in HP 2100A/S Computers or initial binary loader (IBL) in HP 21MX Computers.
- d. Load the diagnostic program, HP part no. 91200-16003. This is an absolute program requiring the BBL, or IBL, to load. Re-roll and store the tape.
- e. Set up the P-register to display on the DISPLAY REGISTER and enter 000003 (octal), the starting address of the diagnostic program. Press STORE on the HP 21MX Computer only, on this and subsequent storage steps for the S- and P-registers.
- f. Set the switch register bits 0 through 5 to the select code of the TV interface card (computer I/O slot of the one card or I/O slot of master card).
- g. Press PRESET, then RUN. The program should halt, displaying 102000 (octal).
- h. Set and store** the switch register bit 0 through 2 for the model number of the computer using the following octal codes:

HP 2100A/S	000000
HP 21MX	000003

**HP 21MX-Series Computers only.

- i. Press RUN. The program will HALT with a display of 102001 (octal).
- j. Set and store* the switch register bit 0 for the scan mode used according to the following codes:

American Scan	Set to 1
European Scan	Set to 0
Non-Standard Scan	Set to 0
- k. Press RUN. The program will halt with a display of 102077 (octal). This is a final halt for initial setup. Proceed to one of the tests below.

4-10. GRAY SCALE OR COLOR

4-11. For all the following tests where gray scale or color operation is used, the switch register bits 0 through 3 must be set for the desired BW or color display. For single BW monitors these bits should be 0 for normal operation. Use one of the codes listed in table 4-1.

Table 4-1. Color and Gray Scale Codes

SW REG. 2-1-0	3-CARD COLOR	3-CARD BW	2-CARD COLOR	2-CARD BW
0-0-0	White	7/8 wh	Yellow	3/4 wh
0-0-1	Black	Black	Black	Black
0-1-0	Red	1/2	Red	1/2
0-1-1	Green	1/4	Green	1/4
1-0-0	Blue	1/8	Black	Black
1-0-1	Yellow	3/4	Yellow	3/4 wh
1-1-0	Magenta	5/8	Red	1/2
1-1-1	Cyan	3/8	Green	1/4

Notes: 1. If black is selected, no pattern will appear on the screen.
 2. Switch register bit 3, when set to 1, reverses video polarity. Refer to table 3-4 for details.

4-12. GO NO-GO TEST

4-13. The go no-go test is a quick operational check of the TV interface card. This test contains subroutines which allow an I/O check, display of the test patterns, and a flashing HP logo. Subsequent steps in the following procedure give the starting addresses of these subroutines. The procedure assumes that the diagnostic test setup specified in paragraph 4-8 has been implemented. The procedure is as follows:

- a. Select the P-register of the computer, enter and store* 00002 (octal).
- b. Select the S-register CLEAR DISPLAY, and change and store* any bits from 0 to 1 for the desired option as follows:

*HP 21MX-Series Computers only.

- Bits 0 thru 3 Color and video polarity (refer to table 4-1).
- Bit 15 If set, test repeats.
- Bit 14 If set, colors will automatically be cycled by incrementing bits 0, 1, and 2 of the switch register giving a new color for each pass. Black is skipped.

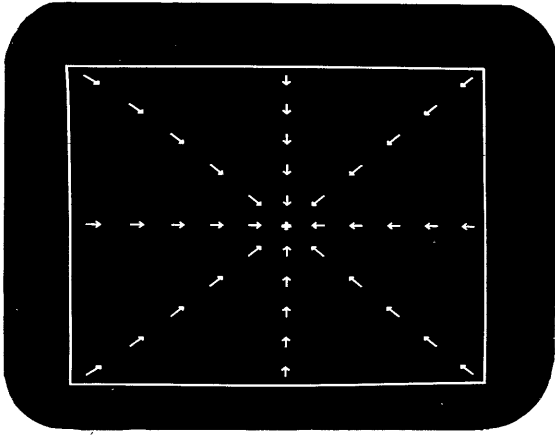
- c. Press PRESET, then RUN.

4-14. The first part of the test checks all I/O instructions. Program halt octal codes showing in the display register indicate the following conditions:

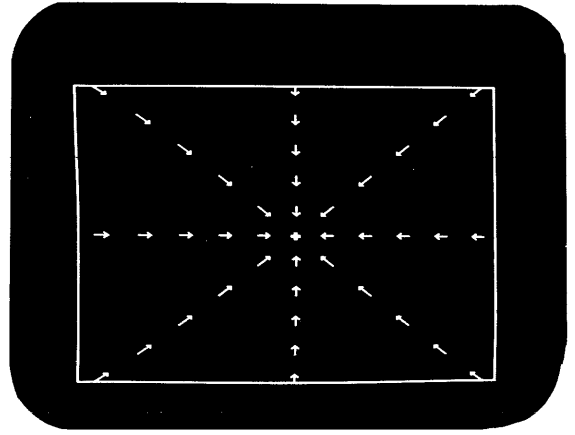
- 102077 Test passed after all patterns displayed and HP logo flashed.
- 102002 Test failed. Indicated bulk erase is not completing.
- 102005 Test failed. Indicates I/O failure according to the code stored in A- and B-registers as follows:
 - 0 — Flag not set, or bad SFS.
 - 1 — SFC bad.
 - 2 — Mode problem, flag not setting at end of mode.
 - 3 — Flag not clearing, or mode not clearing.
 - 4 — SFC bad.
 - 5 — Select code decoding bad (LSB).
 - 6 — Select code decoding bad (MSB).
 - 7 — Priority chain bad in TV card, or interrupt card not installed in next lower priority slot.
 - 10 — No interrupt.
 - 11 — No write response.

Following an error halt 102005 (octal), pushing RUN will cause the I/O check to be repeated without continuing with the other tests.

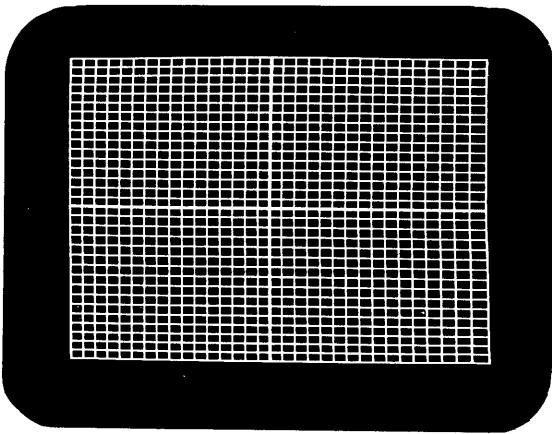
4-15. If no errors are detected, the test continues with pattern displays. Each pattern is held briefly in the following order: gain, crosshatch, settling time, all points, and HP logo. The patterns (except for all points) are shown in figure 4-1. The crosshatch pattern is modified to selectively erase all points in the pattern in the same order as they were written. The all points pattern erases selectively all points of the screen in the opposite order from the writing order.



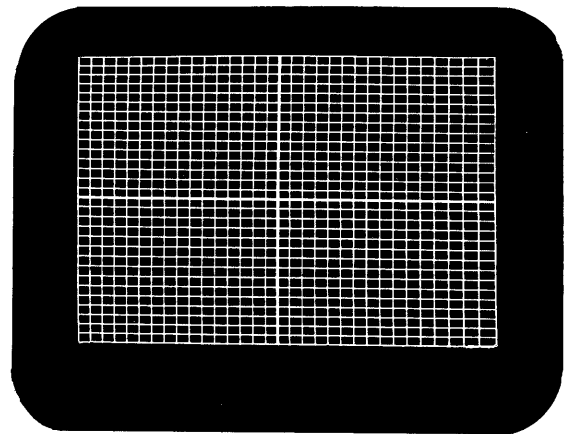
(A) NON-STANDARD & EUROPEAN STANDARD
GAIN TEST PATTERN 256X256



(B) GAIN TEST PATTERN (AMERICAN) 256X240



(C) CROSSHATCH TEST PATTERN
(NON-STD, EUROPEAN) 256X256



(D) CROSSHATCH TEST PATTERN
(AMERICAN STD) 256X240

Figure4-1. Diagnostic Test Patterns

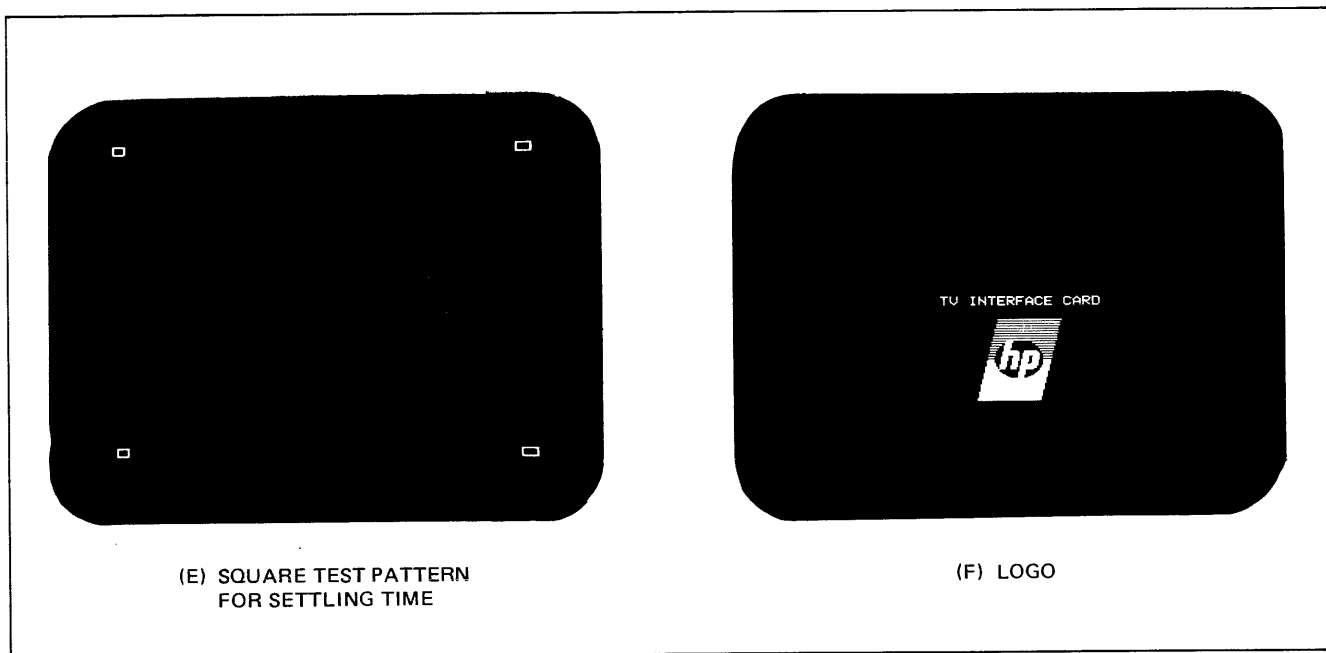


Figure 4-1. Diagnostic Test Patterns (continued)

4-16. After patterns, the test continues with a test of video polarity switching. If white is selected, the HP logo is displayed in white with a black background then changes to black on white. If color was selected, the display first shows the background in the complementary color followed by the logo in the selected color, then the polarity reverses at half the rate of the white-to-black flashing.

4-17. To continuously repeat the I/O check for troubleshooting, set the octal starting address in the P-register to 000103 (octal) and enter 1 in bit 15 of the S-register. Press RUN. To repeat the test only once, set bit 15 in the switch register to 0. The program will start by pressing RUN at this address following a halt 102005 (octal).

4-18. To display patterns only, set the octal starting address in the P-register to 000101 (octal). Press RUN.

4-19. To perform only the video polarity test with the flashing logo, set the octal starting address in the P-register to 000102 (octal). Press RUN.

4-20. SUPER TEST

4-21. The super test provides six different test patterns to allow adjustment of the TV monitor. They will also assist in finding defects in point writing. The patterns may be displayed singly or sequentially at the users discretion. Time delay between sequential patterns is selectable and any one pattern can be continuously flashed in a video polarity reversal mode at a user selected rate. The color may be selected for the patterns at any time. Super test selections and conditions using the computer switch register are listed in table 4-2.

4-22. To run the super test, proceed as follows:

- a. If the program is not already loaded and configured, perform the procedure described in paragraph 4-8.
- b. Set up the starting address 000100 (octal) in the P-register.
- c. Clear the S-register.
- d. Press RUN.
- e. Select the desired test selections and conditions from table 4-2 and enter them in the S-register.
- f. Perform the following test familiarization procedures if desired:
 - (1) Set switch 4 to display the gain test once. See figure 4-1(A) for the 256 by 256 scan and figure 4-1(B) for the 256 by 240 scan.
 - (2) To change the display to the crosshatch test pattern, set switch 5. This display is shown in figures 4-1(C) and (D) for the two different scan modes.
 - (3) Set switches 6 through 8, one after the other, to view the remainder of the displays.
 - (4) To repeat a pattern, or patterns, continuously with approximately 5 seconds delay between patterns, set switch 15 then the switches for the test patterns desired.
 - (5) To shorten the delay time between patterns to about 1 second, set switch 13.

Table 4-2. Super Test Selections and Conditions

SWITCH REGISTER OPTIONS:		
TEST CONDITIONS		
SW NO.	SETTING	ACTION
0-2*	—	Color or Gray Scale selection as given in table 4-1.
3*	0	Video polarity normal.
	1	Video polarity inverted.
15	0	Individual test occurs once when test switch set to 1**. Tests continue, showing patterns selected by switches 4-8, and repeat at intervals set by time delay (switches 11-13 below).
	1	
14	0	Tests continue.
	1	Halt 102077 (octal) at end of test (super test may be restarted by pressing RUN). This bit will clear upon halt.
13*	0	Time delay is about 5 seconds unless switch 12 is set.
	1	Time delay is about 1 second unless switch 12 is set.
12*	0	Time delay is selected by switch 13.
	1	Time delay is less than 1 second.
11*	0	Standard time delays.
	1	Repetition speed-up (about 3 times faster).
10	0	Normal operation.
	1	Alternating video polarity (flashing pattern) at the rate set by switches 11-13, if switch 15 is 0.
TEST		
Switches 4-8 select the test:		
4	GAIN	Approximate gain, position, and focus adjust. A square or rectangle is drawn around the circumference of the TV (256 x 256 or 256 x 240), enclosing a pattern of arrows pointing to the center. Shown in figures 4-1(A) and (B).
5	CROSS	Crosshatch for precision adjustments. A grid of horizontal and vertical lines are drawn covering the entire TV screen. The center lines are heavy, allowing adjustment of position. Shown in figures 4-1(C) and (D).
6	ALL PTS	All Points Test. All matrix points are written.
7	SQUARES	Corner and Settling Time Test. An 8 x 8 square is drawn in each of the four corners of the TV screen. Shown in figure 4-1(E).
8	LOGO	Writes title with HP logo. Shown in figure 4-1(F).
9	BLANK	Erases screen.
*Can be changed at any time. Takes effect on next generated pattern.		
**Test switch clears automatically.		
Note: HALT 102002 (octal) indicates that the erase time exceeded the specification. You may proceed by pressing RUN.		

- (6) To shorten the delay times to less than 1 second, set switch 12. Note that switch 12 overrides switch 13.
- (7) For minimum delay, set switches 11 and 12.

4-23. A combination of patterns is usually desired for TV monitor adjustment. A typical method using the super test is as follows:

- a. Gain pattern — to adjust the controls for monitor gain position, and focus.
- b. Crosshatch pattern — to adjust pattern curvature (pin cushion), linearity, and color monitor convergence.
- c. All points test — to determine if all points are being written and to check sync capability by immediately setting another test switch to see if sync is momentarily lost. If sync is marginal, possibly external sync should be considered.
- d. Settling time pattern (squares in corners) — to check monitor settling time (if specified by TV monitor manufacturer).
- e. Check of the inverting video polarity writing capability by selecting the appropriate test condition (switch 3 set to 1).

4-24. RAM TEST

4-25. The random access memory (RAM) test allows the test of RAM's individually. The super test, described under paragraph 4-20, allows writing of all matrix points. Thus, if a point is detected in the super test as not being written or erased, the malfunctioning RAM may be quickly identified. In the super test pattern, the unwritten point may be marked with a grease pencil to locate it during the RAM test. In this test, each RAM is addressed individually and the resultant display is comprised of 16 vertical lines positioned according to the locations written by that particular RAM. Absence of a line, or part of it identifies a faulty RAM.

4-26. There are 16 RAM's numbered from 0 through 17 (octal) to cover 256 horizontal points. RAM 0 contains all points with horizontal (X) addresses of 0,16,32 . . . to 240 with 0 being furthest on the left side of the screen. RAM 1 contains all points with horizontal (X) addresses of 1,17,33 . . . to 241. Similarly RAM's 2 through 17 cover the remaining addresses with RAM 17 containing all points with horizontal (X) addresses of 15,31,63 . . . to 255.

4-27. The procedure for operating the RAM test is as follows:

- a. If the program is not already loaded and configured, perform the procedure specified in paragraph 4-8.
- b. Enter the starting address of 002000 (octal) in the P-register.

- c. Set the RAM number desired from 0 through 17 (octal) (as described above) in switch register bits 12 through 15; e.g., 120000 (octal).
- d. For color, set bits 0 through 2, according to table 4-1, in the switch register along with the RAM number.
- e. Press PRESET, then RUN. A halt is always observed — for convenience the halt code contains the RAM number selected; e.g., 102012 (octal) for RAM 12 (octal). Normally, this will display all points of 16 vertical lines.

Note: HALT 102002 (octal) may indicate that the erase time exceeded specification if RAM 2 were not programmed and the RAM pattern was not displayed. To distinguish from RAM 2, try another RAM. Proceed by pressing RUN.

- f. Press RUN again. Observe a HALT with all points in the selected RAM selectively erased. The halt code will agree with the RAM selected.
- g. Repeat steps c,d,e, and f until all RAM's have been checked or a faulty RAM isolated. The RAM number (octal 0 through 17) in this procedure corresponds with the RAM numbers shown in figure 2-1.

4-28. COLOR BAR TEST

4-29. For multicard systems, all colors (or all levels of gray) can be displayed in a bar pattern. The pattern is shown in figure 4-2(A) for three cards and 4-2(B) for two cards. Each bar is a different color (or gray level) with black on the left and white on the right as labeled on the bars in figure 4-2. If this pattern is selected for a one-card system, the screen is black on the left half and white on the right half and lower portion. To select the color bar pattern, proceed as follows:

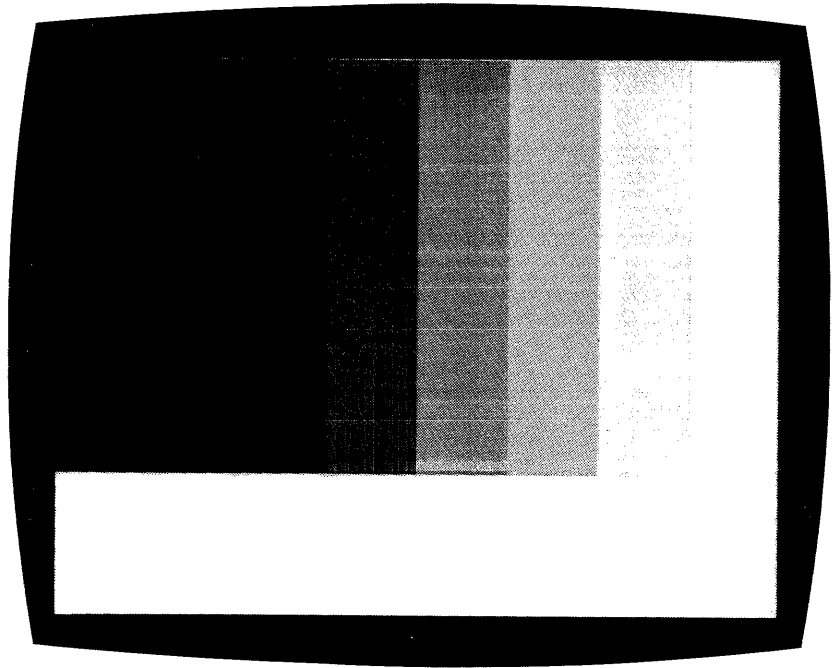
- a. Enter the starting address of 000104 (octal) into the P-register.
- b. Set bits into the switch register the same as in the super test for switch register bits 15,13,12,11, and 10, if repeating or flashing of the pattern is desired.

4-30. The color bar pattern can be used for setting tint controls on color monitors or for setting the three adjustment controls on the TV interface master card for multi-level gray. Also the black-and-white monitor can be adjusted for contrast and brightness.

4-31. HP 2100A/S COMPUTER BBL

4-32. The Basic Binary Loader (BBL) is a sequence of instructions which will load, into the computer memory, programs prepared with absolute addresses, using defined input devices. The instructions are stored in the highest

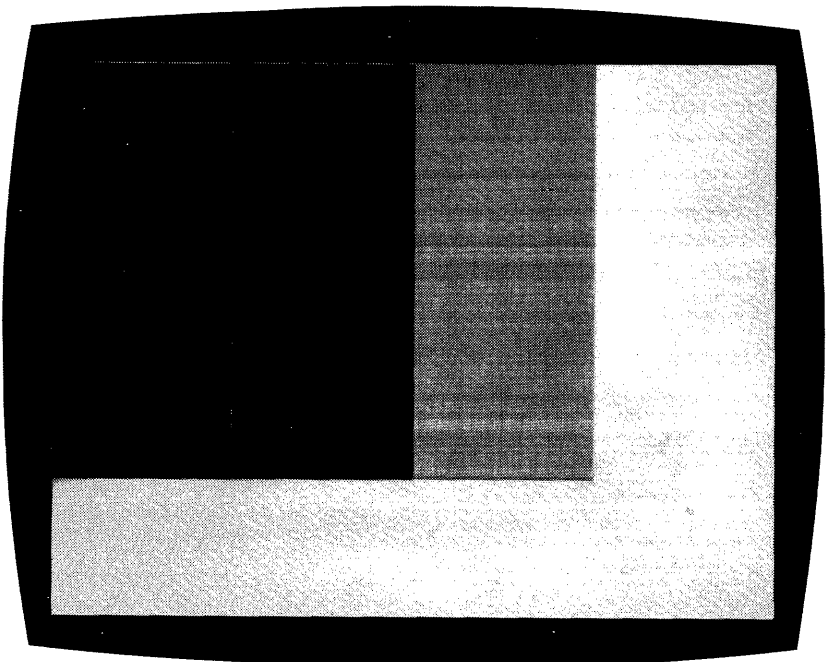
COLOR	BLACK	BLU	GRN	CYN	RED	MAG	YEL	WHT
GRAY LEVEL	BLACK	1/8	1/4	3/8	1/2	5/8	3/4	7/8



7202-5A

(A) BAR DISPLAY FOR THREE TV INTERFACE CARDS

COLOR	BLACK	GREEN	RED	YELLOW
GRAY LEVEL	BLACK	1/4	1/2	3/4



7202-5B

(B) BAR DISPLAY FOR TWO TV INTERFACE CARDS

Figure 4-2. Color Bar or Multilevel Gray Test Pattern

64 memory locations of your computer. Whenever you encounter a procedure directing the use of the Basic Binary Loader to load an absolute binary tape, use the procedure described here. The procedure will identify the particular tape to be loaded.

4-33. The standard input device for these procedures will be a high-speed tape reader or the teleprinter tape reader (no high-speed tape reader in the system). Loading is accomplished as follows:

- a. Turn on the input device and prepare for reading (e.g., load tape in tape reader). The input program must be in binary form, containing absolute addresses.
- b. Press S to select the S-register. This will cause the S-register contents to be displayed in the DISPLAY REGISTER.
- c. Clear bits 0 and 15 of the display. (These bits are to be set only for certain nonloading check operations; refer to software operating manual.) The status of the remaining bits is not significant.
- d. Press P to select the P-register. This will cause the P-register contents to be displayed in the DISPLAY REGISTER.
- e. Set the display to the starting address of the basic binary loader, according to table 4-3.

Table 4-3. Starting Address for Basic Binary Loader

MEMORY SIZE	OCTAL STARTING ADDRESS
4K	07700
8K	17700
12K	27700
16K	37700
24K	57700
32K	77700

- f. Press EXTERNAL PRESET and INTERNAL PRESET. This initializes the external hardware (I/O channels) and the internal hardware (central processor).
- g. Press LOADER ENABLE, and then press RUN. The lights for both switches will remain on while the input operation is in progress.
- h. When the input device stops, the HALT light will go on, RUN and LOADER ENABLE lights will go off, and the DISPLAY REGISTER should indicate 102077 (octal), with MEMORY DATA automatically selected. The load is complete.

4-34. HP 21MX COMPUTER IBL

4-35. This procedure describes a cold start using the standard paper tape loader ROM, which will allow a pro-

gram to be loaded via a punched-tape reader. At the rear of the computer, set the ~ LINE and BATTERY switches to ON and proceed as follows:

- a. On the operator panel, set key-operated switch to OPERATE.
- b. Press left half (◀) or right half (▶) of Register Select switch to select S-register.
- c. Press CLEAR DISPLAY and set bits 6 through 11 to display octal select code of tape reader.
- d. Set bits 15 and 14 to zeros to select standard paper tape loader ROM.
- e. Press STORE and then press IBL. The paper tape loader is now loaded into the uppermost 64 locations of memory and the select code of the tape reader is patched according to the contents of the S-register. The P-register is now pointing to the first instruction of the loader.
- f. Turn on tape reader and prepare it for reading. Press PRESET and then press RUN. The program will now be read into memory and the computer will halt with the T-register selected automatically. A successful load is indicated if the Display Register contents are 102077 (octal).

To run a program after it has been loaded, proceed as follows:

- a. Press left half (◀) or right half (▶) of Register Select switch to select P-register.
- b. Press CLEAR DISPLAY and set Display Register to starting address of program.
- c. Press STORE, PRESET, and RUN.

The RUN indicator will remain lighted as long as the program is running. If the key-operated switch is set to OPERATE, all operator panel controls except the Display Register, CLEAR DISPLAY, and HALT switches are disabled. The S-register is displayed automatically and can be changed manually via the Display Register bit switches. If the key-operated switch is set to LOCK, the RUN and HALT switches are disabled and all other switches are enabled within the constraints of the run and halt modes.

4-36. ERROR HALTS

4-37. If the halt code is not 102077 (octal) when the device stops, there has been an error in the loading process. Two possible error conditions are indicated by the loader, which changes the halt code to identify the type of error. A halt code of 102055 (octal) indicates an address error, check if the proper tape is being read, or if it is in backwards. A halt code of 102011 (octal) indicates a checksum error; check for possible bad tape, or dirty tape reader or tape.



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